

Airking_JL

Schematics Document

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Hynix 4G EMMC

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Title

Cover Page

Size
A4

Document Number

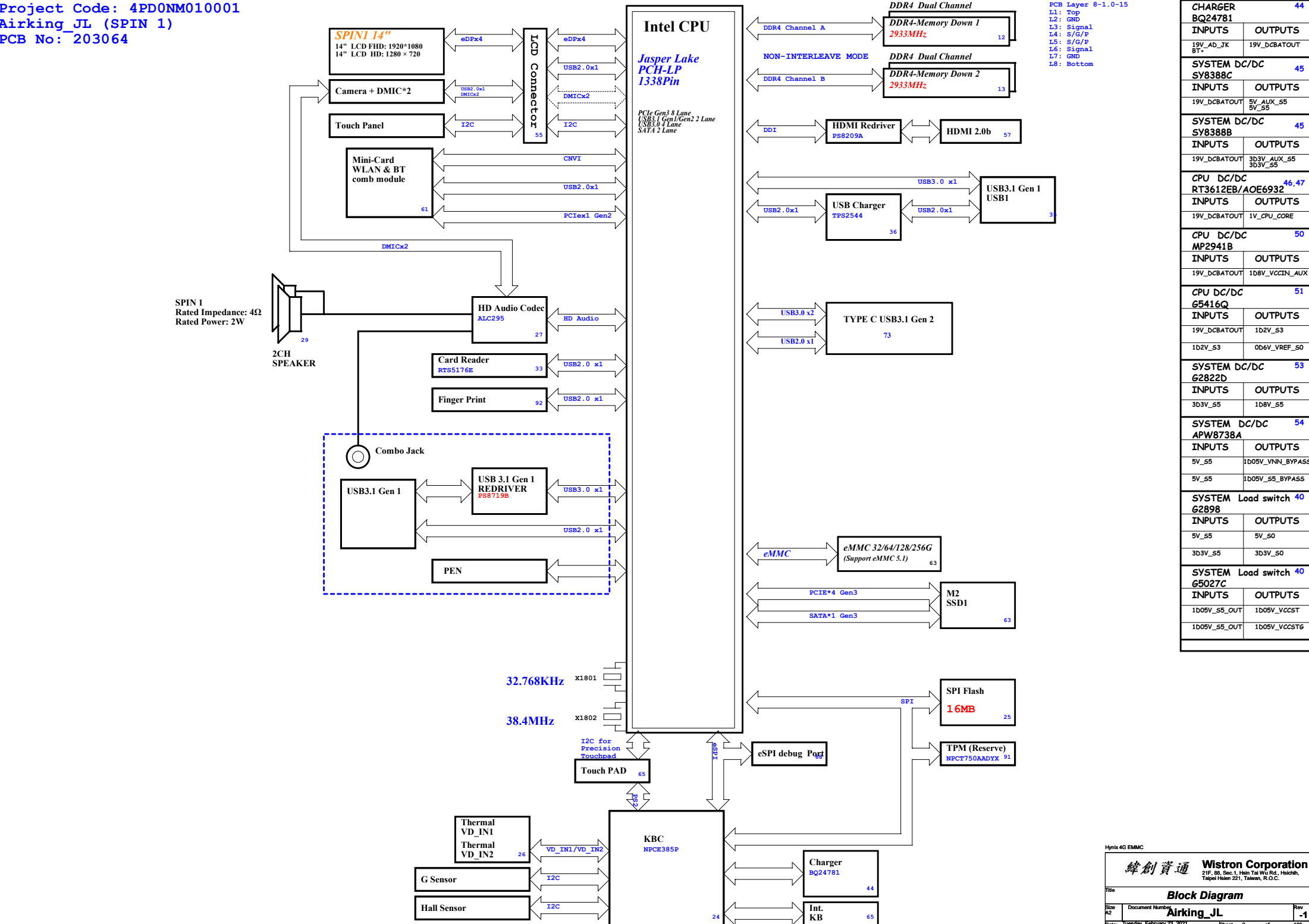
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Rev
-1

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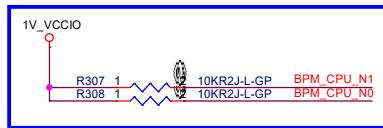
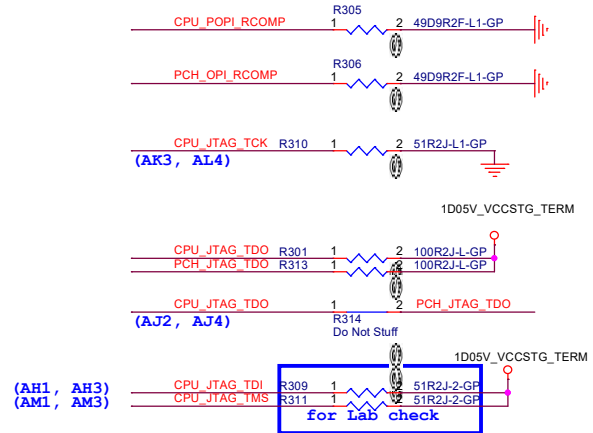
Sheet 1 of 106

Project Code: 4PD0NM010001
Airinging_JL (SPIN 1)
PCB No: 203064

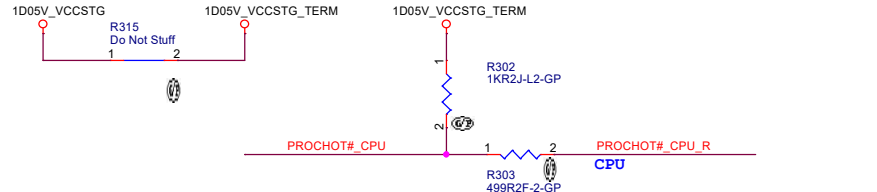


Hynix 4G EMMC

15	DBG_PMODE	<<—
24,44,46	PROCHOT#_CPU	<<—>>—
46	SVID_ALERT#_CPU	>>—>>—
46	SVID_DATA_CPU	<<—<<—
46	SVID_CLK_CPU	<<—<<—
89	CPU_JTAG_TRST#	<<—



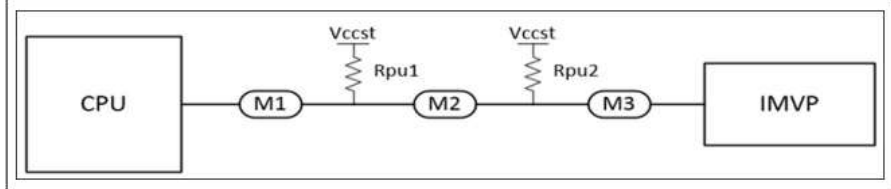
The diagram illustrates a multi-agent system architecture. It features a sequence of modules (M0 through M10) connected in a line. Each module Mi is connected to a corresponding agent (Agent 1 through Agent 5) via a resistor Ri. The agents are connected to a common ground. The diagram also shows a 'VccSTG' supply connected to the first module M0 and a 'VccSTG' supply connected to the last module M9. The diagram includes the following text: 'Runstuff Placeholder', 'VccSTG', 'R0=1kOhm', 'R1=500Ohm', '200 Ohm > Ri + RAgent > 75 Ohm', '200 Ohm > R0 + RAgent > 75 Ohm', 'Inv OD', 'M10', 'EC', and 'CPU'.



100R2J-L-GP R316

1D05V_VCCST

SVID_DATA_CPU



SVID_DATA platform resistors	Rpu1=100Ω, Rpu2=100Ω
SVID_CLK platform resistors	Rpu1=Empty, Rpu2=45Ω
SVID_ALERT_N platform resistors	Rpu1=56Ω, Rpu2=Empty
Platform resistors tolerances	5%
Route ordering	When routing at minimum spacing route Alert between Data and Clock

eDP

55 eDP_TX_CPU_P0
55 eDP_TX_CPU_N0
55 eDP_TX_CPU_P1
55 eDP_TX_CPU_N1
55 eDP_TX_CPU_P2
55 eDP_TX_CPU_N2
55 eDP_TX_CPU_P3
55 eDP_TX_CPU_N3
55 eDP_AUX_CPU_P
55 eDP_AUX_CPU_N

55 eDP_HPD_CPU

55 eDP_BKLTCTL_CPU
24 eDP_BKLTEN_CPU
55 eDP_VDDEN_CPU

HDMI

57 HDMI_DDI_TX_P2
57 HDMI_DDI_TX_N2
57 HDMI_DDI_TX_P1
57 HDMI_DDI_TX_N1
57 HDMI_DDI_TX_P0
57 HDMI_DDI_TX_N0
57 HDMI_DDI_TX_P3
57 HDMI_DDI_TX_N3

57 HDMI_SCL_CPU
15,57 HDMI_SDA_CPU

57 HDMI_DET_CPU

15 GP_E14
15 GP_E18
15 GP_A15

24 ME_UNLOCK

eDP

eDP_TX_CPU_P0 F6
eDP_TX_CPU_N0 G7
eDP_TX_CPU_P1 E5
eDP_TX_CPU_N1 D4
eDP_TX_CPU_P2 H6
eDP_TX_CPU_N2 J5
eDP_TX_CPU_P3 J8
eDP_TX_CPU_N3 J7
eDP_AUX_CPU_P F9
eDP_AUX_CPU_N E10

HDMI

HDMI_DDI_TX_P2 L4
HDMI_DDI_TX_N2 M2
HDMI_DDI_TX_P1 H3
HDMI_DDI_TX_N1 H4
HDMI_DDI_TX_P0 J4
HDMI_DDI_TX_N0 J2
HDMI_DDI_TX_P3 F3
HDMI_DDI_TX_N3 G1

K1
K3

E12
D11
C10
D10
B7
A7
C8
A8
B9
D8

CPU1A

JSL-CELERON-QC-GP-U

ZZ.00CPU.521

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DDI0_TXP0
DDI0_TXN0
DDI0_TXP1
DDI0_TXN1
DDI0_TXP2
DDI0_TXN2
DDI0_TXP3
DDI0_TXN3
DDI0_AUXP
DDI0_AUXN
DDI1_TXP0
DDI1_TXN0
DDI1_TXP1
DDI1_TXN1
DDI1_TXP2
DDI1_TXN2
DDI1_TXP3
DDI1_TXN3
DDI1_AUXP
DDI1_AUXN
DDI2_TXP0
DDI2_TXN0
DDI2_TXP1
DDI2_TXN1
DDI2_TXP2
DDI2_TXN2
DDI2_TXP3
DDI2_TXN3
DDI2_AUXP
DDI2_AUXN

EDP_BKLTCTL
EDP_BKLTEN
EDP_VDDEN
EDP_DISP_UTIL/MDSI_DE_TE_1
MDSI_DE_TE_2

GP_E13/DDI0_DDC_SCL
GP_E14/DDI0_DDC_SDA
GP_A17/DDI0_HPD

GP_E15/DDI1_DDC_SCL
GP_E16/DDI1_DDC_SDA
GP_A16/DDI1_HPD/TIME_SYNC_1

GP_E17/DDI2_DDC_SCL
GP_E18/DDI2_DDC_SDA
GP_A15

DISP_RCOMP
RSVD_TP_27

CC15 eDP_BKLTCTL_CPU
CB17 eDP_BKLTEN_CPU
CC17 eDP_VDDEN_CPU

AA4
W2

CL6
CM5
CM30

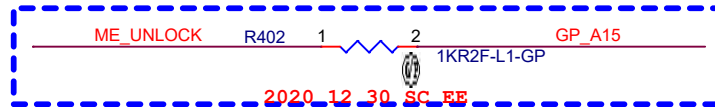
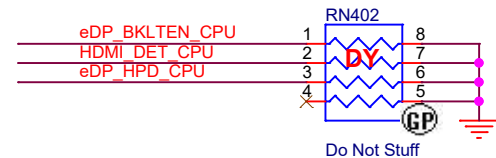
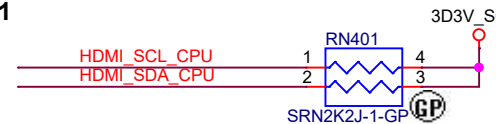
CK5
CN4
CN29

CF7
CF5
CP29

E3 DISP_RCOMP

E1

1 2
R401
150R2F-4-L-GP



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Title

CPU (DDI/eDP)

Size

Document Number

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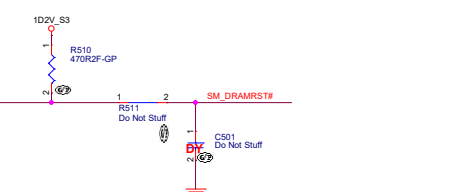
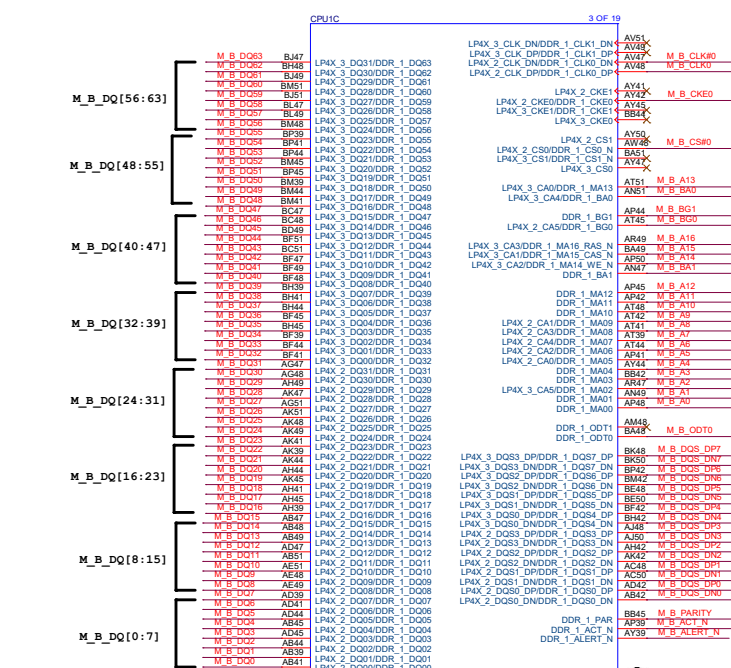
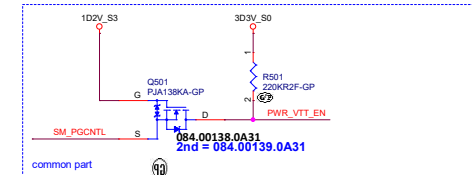
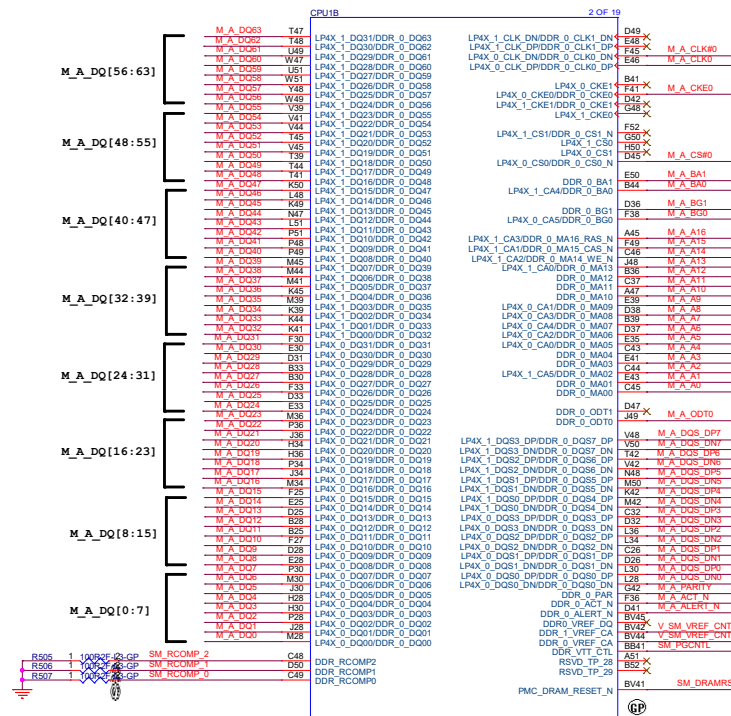
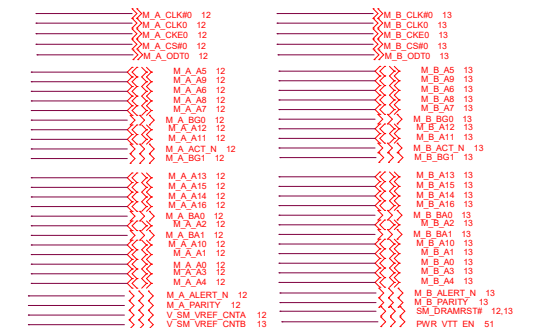
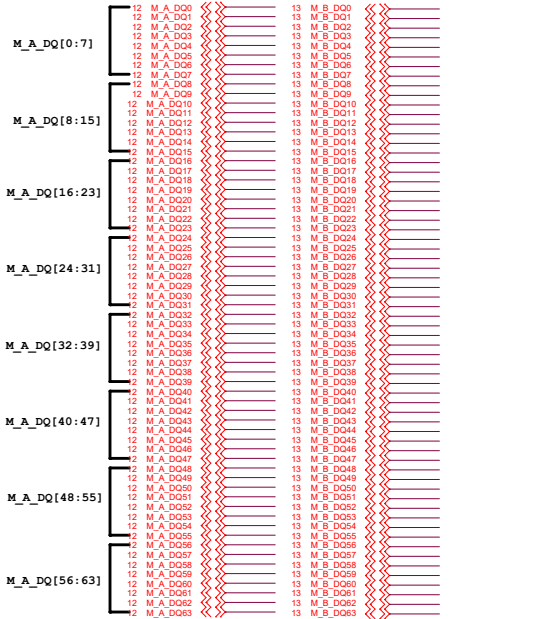
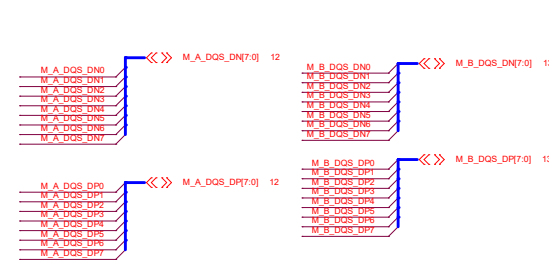
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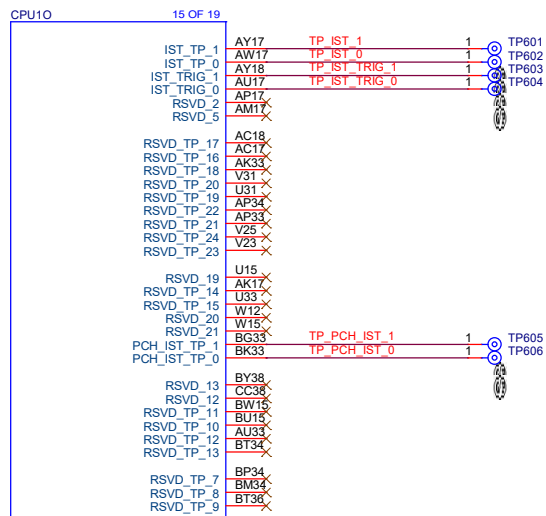
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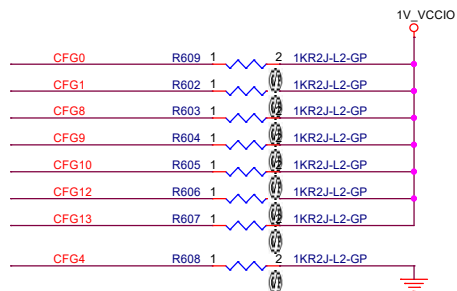
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DDR4 ball type: Non-Interleaved



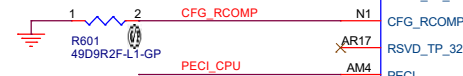
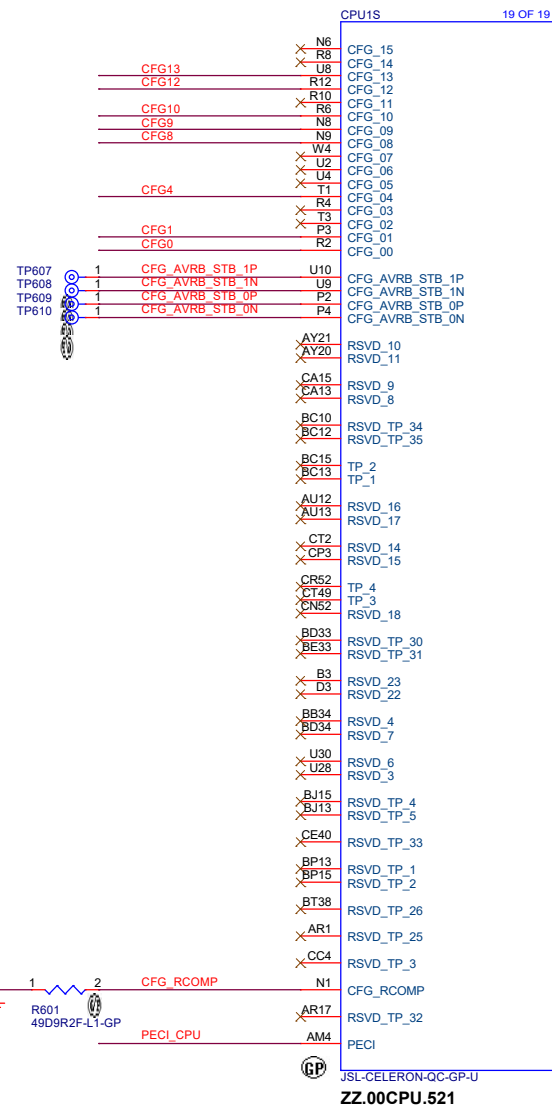
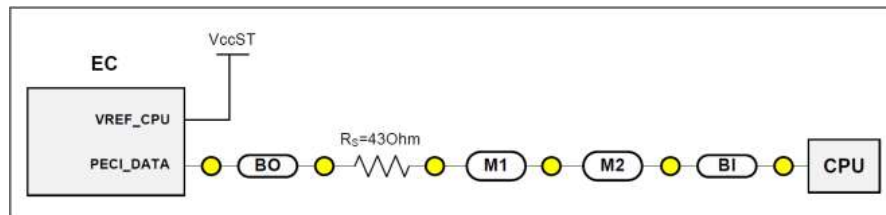


ZZ.00CPU.521



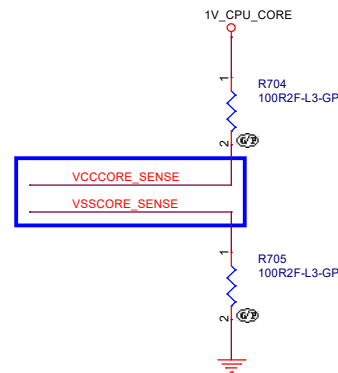
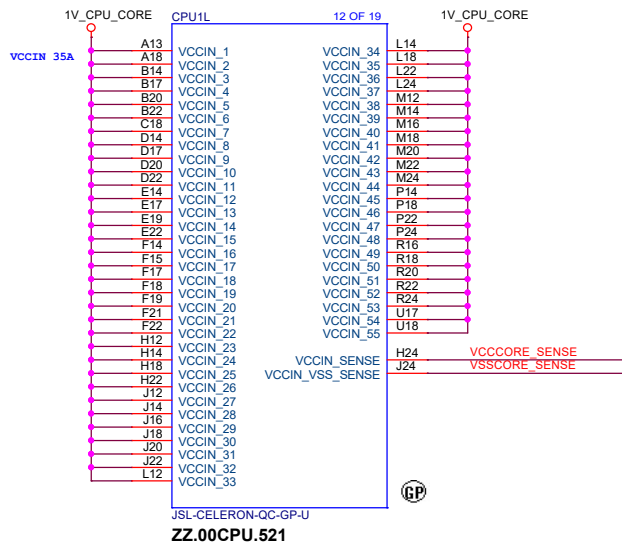
Document Number: 613095 Ver 1.1

CFG	Description	Termination	Resistor
CFG0	CFG[0]: Stall reset sequence after PCU PLL lock until de-asserted: — 1 = (Default) Normal Operation; No stall. — 0 = Stall.	Pull Up to VCCIO_EXT	1K Ohm
CFG1,8,9,10,12,13	RSVD	Pull Up to VCCIO_EXT	1K Ohm
CFG2,3,5,6,7,11,14,15	RSVD	No termination	N/A
CFG4	CFG[4]: eDP enable: — 1 = Disabled. — 0 = Enabled.	Pull Down	1K Ohm



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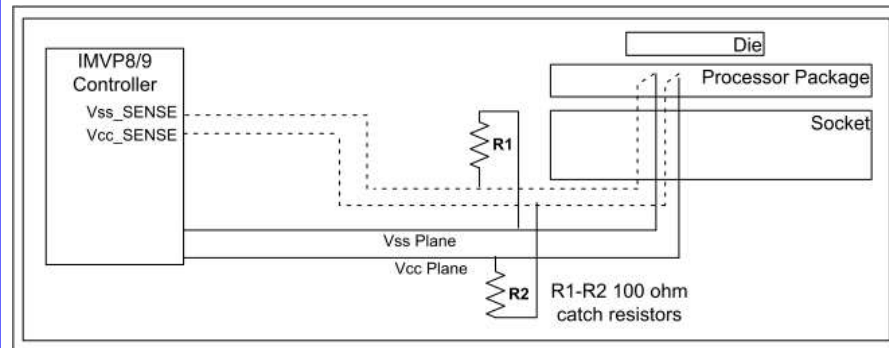
46 VCCCORE_SENSE
46 VSSCORE_SENSE



Document Number: 613095 Ver 0.9

– R1, R2 should be placed within 2 inches (50.8 mm) of the processor socket, minimizing any potential error due to Vcc_SENSE/Vss_SENSE line resistance.

– Preserve the transmission line integrity of Vcc_SENSE/Vss_SENSE lines by avoiding stub routing to R1, R2 catch resistors.



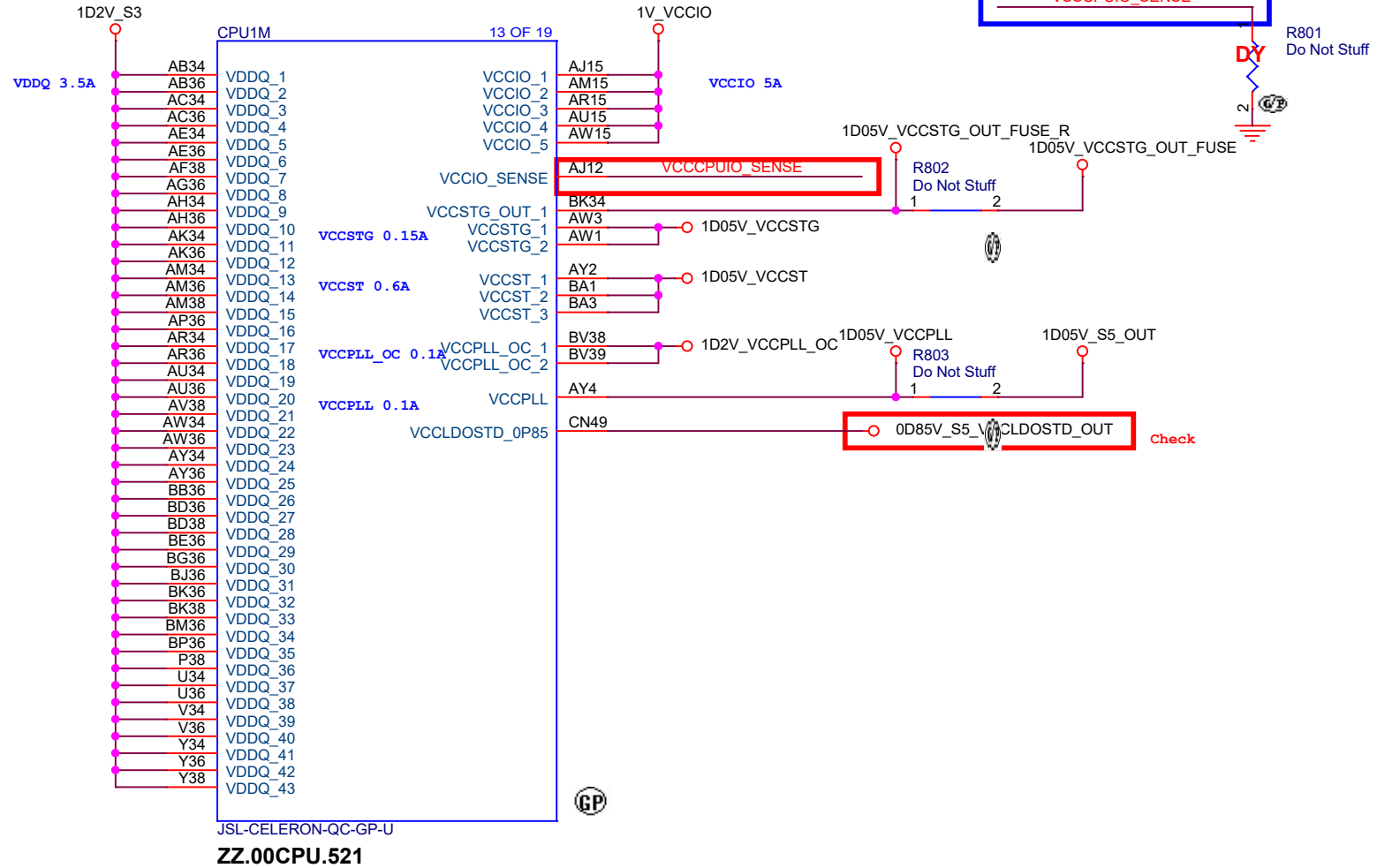
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Title			CPU (VCCIN)	
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54 VCCCPUIO_SENSE
54 VSSCPUIO_SENSE



JSL-CELERON-QC-GP-U
ZZ.00CPU.521

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Title			CPU (VDDQ/VCCIO)	
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A4	Airking_JL		-1	
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SizeA4	Document NumberAirking_JL	Rev-1
Date: Tuesday, February 23, 2021	Sheet 9 of	106

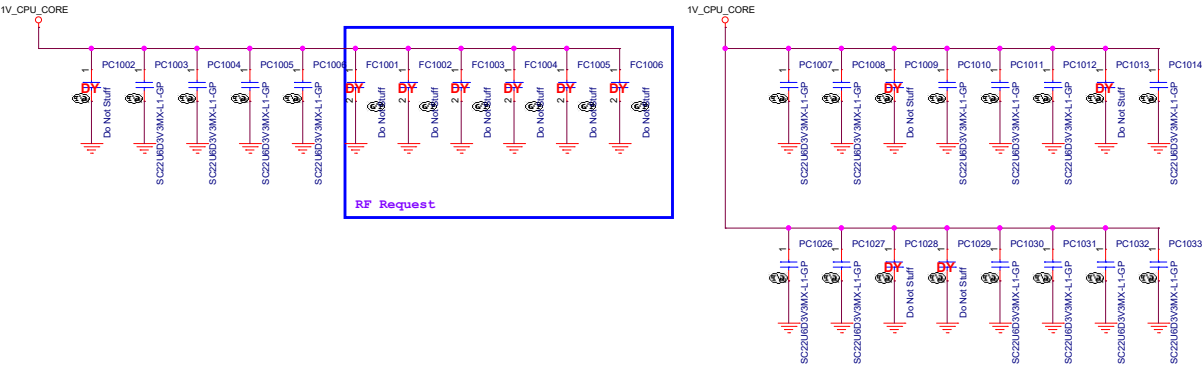
Main Func = CPU

JSL_6W

VCORE

IccMax current-10ms max = 33 A

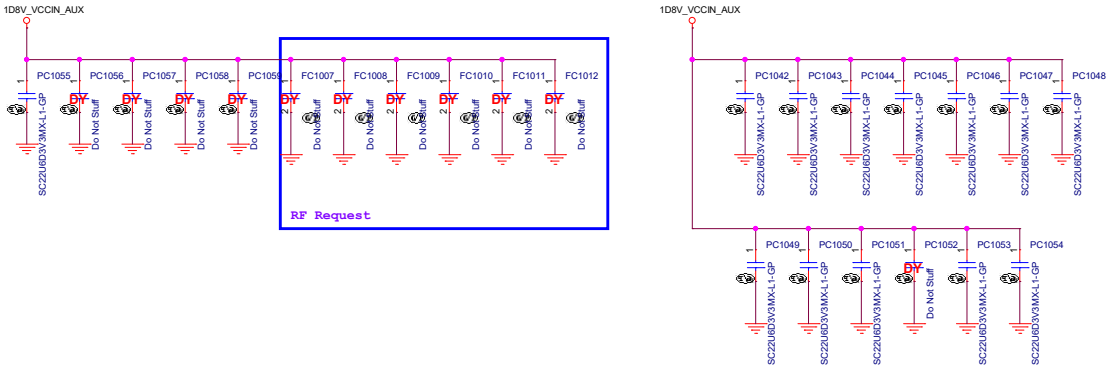
22uF	PCS	Cap
JSL_6W	21	330uF*1



VCCINAUX

IccMax current-10ms max = 24 A

22uF	PCS	Cap
JSL_6W	13	330uF*1





Domain	Primary Side Cap	Secondary Side Cap	Placement Guideline
VDDQ	3 x 0603_22uF	2 x 0201_0.1uF 2 x 0402_4.7uF 2 x 0402_10uF	Secondary Side Cap: Place the secondary caps on the bottom power plane and equally distribute, with the highest cap values closer to the VR. Also place the caps beside or as close as possible to the PTHs that connects to the VDDQ BGAs.
Bulk Decoupling Locations		Capacitors	
VDDQ Power Plane at VR output		13 x 0603_22uF Notes: 1. VR share MLCC with PI 2. 3 x 0603_22uF is captured in Table 283 on page 412	
Domain	Primary Side Cap	Secondary Side Cap	Placement Guideline
VCCIO_EXT	12 x 0402_10uF 4 x 0603_22uF	4 x 0402_10uF	
Bulk Decoupling Locations		Capacitors	
VCCIO_EXT Power Plane at VR output		0 x 0603_22uF Notes: 1. VR share MLCC with PI 2. 6 x 0603_22uF is captured in Table 281 on page 410, note that PI only has 4x0603_22uF but the 12x0402_10uF is enough to share with VR	
Domain	Primary Side Cap	Secondary Side Cap	Placement Guideline
VCCSTG	1 x 0402_1uF	None	Place as close as possible to package BGAs, <10mm.
Domain	Primary Side Cap	Secondary Side Cap	Placement Guideline
VCCST	1 x 0402_1uF	None	Place as close as possible to package BGAs, <10mm.
Domain	Primary Side Cap	Secondary Side Cap	Placement Guideline
VCCPLL_OC	1 x 0402_1uF	None	Place as close as possible to package BGAs, <10mm.
Domain	Primary Side Cap	Secondary Side Cap	Placement Guideline
VCCPLL	1 x 0402_1uF	None	Place as close as possible to package BGAs, <10mm.
Domain	Primary Side Cap	Secondary Side Cap	Placement Guideline
VCCLDOSTD_0P85	1 x 0402_2.2uF	None	Place the capacitor <9mm from the package edge.

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Title

CPU (Power Cap2)

Size A3

Document Number

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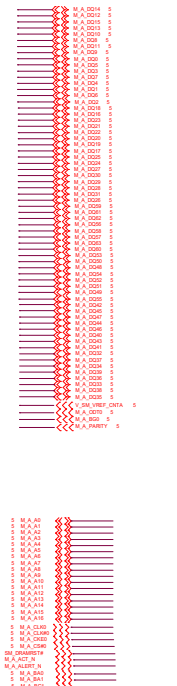
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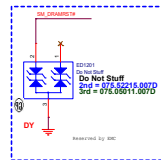
Date: Tuesday, February 23, 2021

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SSID = DDR4 CHA



DQS0	DQ0~DQ7
DQS1	DQ8~DQ15
DQS2	DQ16~DQ23
DQS3	DQ24~DQ31
DQS4	DQ32~DQ39
DQS5	DQ40~DQ47
DQS6	DQ48~DQ55
DQS7	DQ56~DQ63



SDP & DDP SETTING

DDP: 240 ohm
SDP: 0 ohm



DDP x16 and SDP x16 Compatible Layout

- ▶ Alternate two layout, risk of VSS offset increases a little

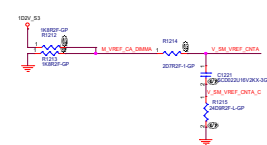
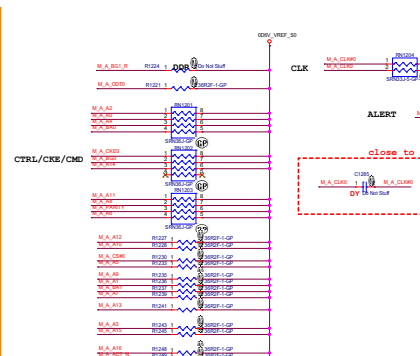
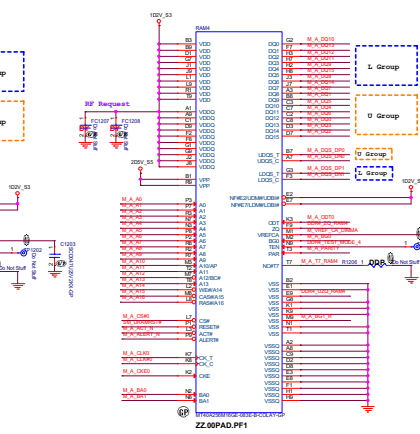
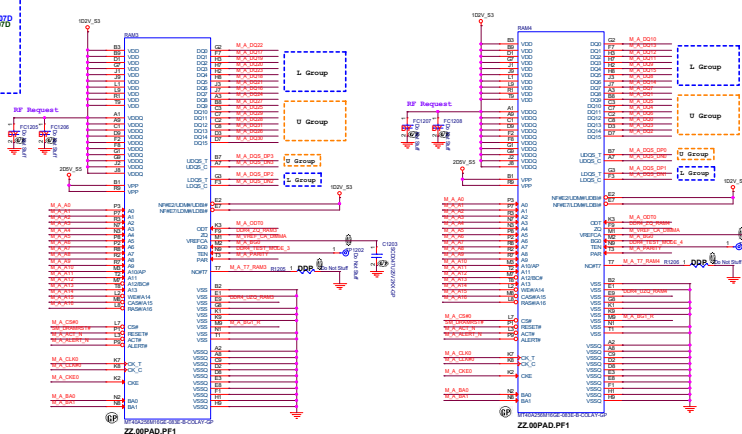
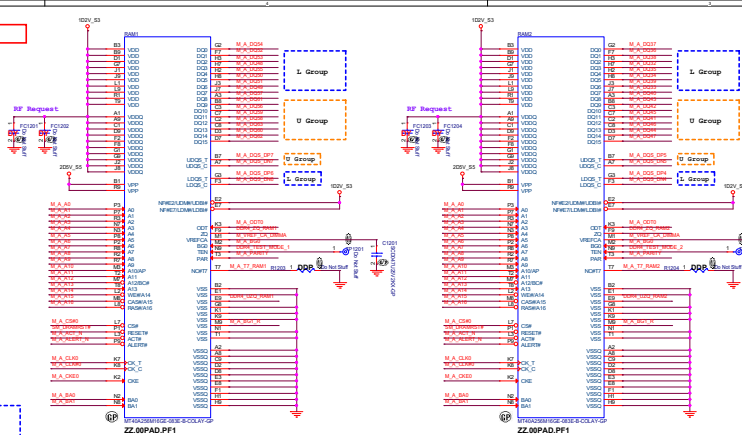
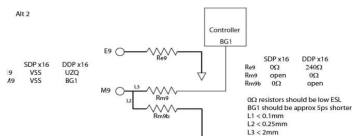


Figure 3-7: RCOMP Topology

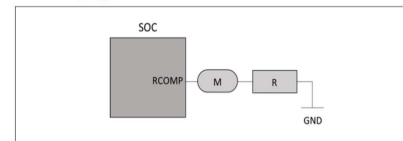
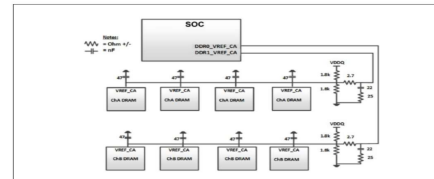


Figure 3-8: DDR4 MD VREF-CA Overview



Memory Configuration	Power Domain	Decoupling Location	Qty x μF (Size)
DDR4 Memory Down to 14 Devices per Channel	VDDQ/VDD	4 per dram, as close as possible. Distribute evenly across domain, close by Drams.	32x 1 μF (4002) 10x 10 μF (6003)
	VPP	2 per dram, as close as possible. Distribute evenly across domain, close by Drams.	5x 1 μF (4002) 16x 1 μF (6003)
	VTT	Distributed along termination resistors.	16x 1 μF (4002)
		Distribute evenly across domain.	4x 10 μF (6003)

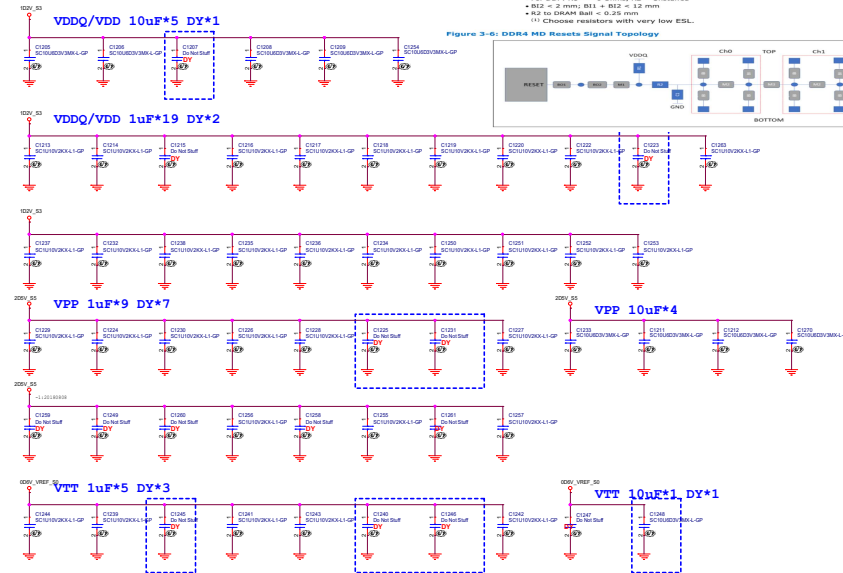


Figure 3-1: DDR4 MD Strobe/Data Signal Topology



Figure 3-2: DDR4 MD CLK Signal Topology

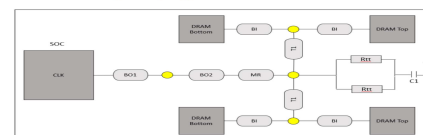


Figure 3-3: DDR4 MD CMD/CTRL Signal Topolog

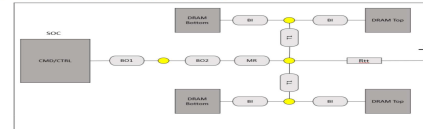


Figure 3-4: DDR4 MD ALERT Signal Topolog

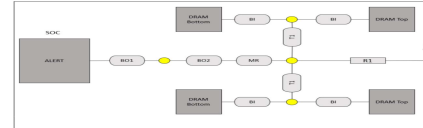
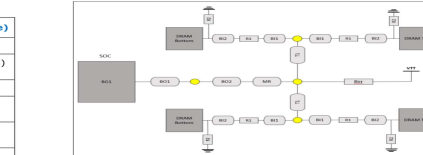


Figure 3-5: BG1 Topology for SDP-DDP Compatibility



NOTE: For BG1 compatibility across SDP and DDP x16 devices:

- For SDP: $R1 = \text{Unstuffed}$, $R2^{(1)} = 0 \text{ Ohm}$
- For DDP: $R1^{(1)} = 0 \text{ Ohms}$, $R2 = \text{Unstuffed}$
- $B12 \leq 2 \text{ mm}$; $B11 + B12 \leq 12 \text{ mm}$
- $R2$ to DRAM Ball $\leq 0.25 \text{ mm}$

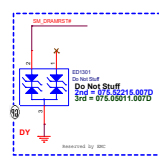
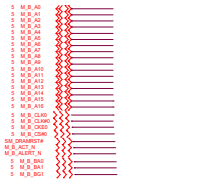
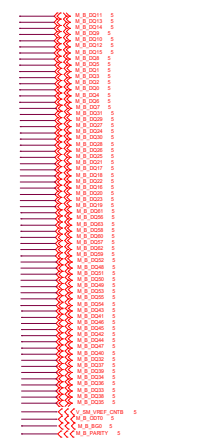
⁽¹⁾ Choose resistors with very low ESL.

Figure 3-6: DDR4 MD Resets Signal Topology



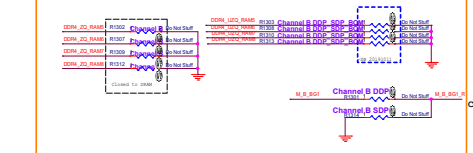
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DQ80	DQ0-DQ7
DQ81	DQ8-DQ15
DQ82	DQ16-DQ23
DQ83	DQ24-DQ31
DQ84	DQ32-DQ39
DQ85	DQ40-DQ47
DQ86	DQ48-DQ55
DQ87	DQ56-DQ63



SDP & DDP SETTING

DDP: 240 ohm
SDP: 0 ohm



DDP x16 and SDP x16 Compatible Layout

• Alternate two layout, risk of VSS offset increases a little

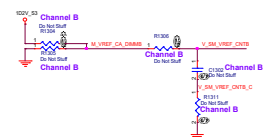
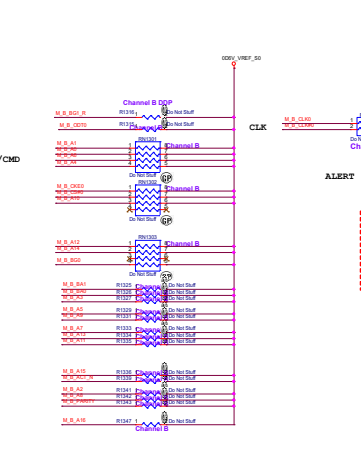
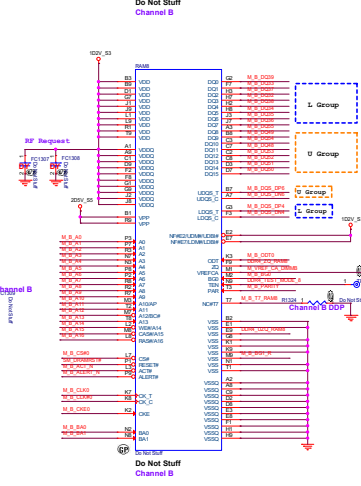
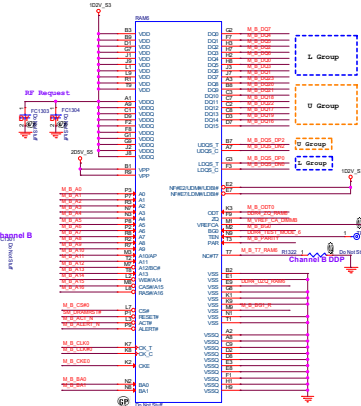
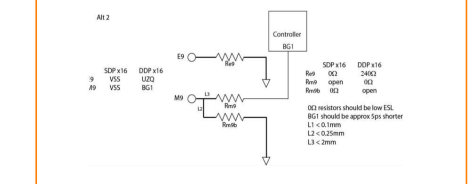


Figure 3-7: RCOMP Topology

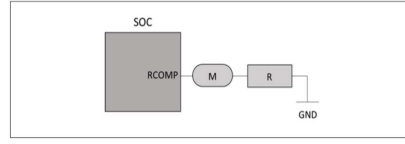
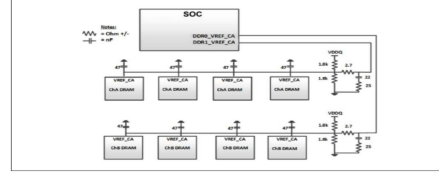


Figure 3-8: DDR4 MD VREF-CA Overview



Memory Configuration	Power Domain	Decoupling Location	Qty x μF (Size)
DDR4 Memory Down x16 - 4 Devices per Channel. Numbers of decoupling capacitors are total for both channels	VDDQ/VDD	4 per dram, as close as possible. Distribute evenly across domain, close by Drams.	32x 1 μF (0402) 10x 10 μF (0603)
	VPP	2 per dram, as close as possible. Distribute evenly across domain, close by Drams.	16x 1 μF (0402) 5x 10 μF (0603)
	VTT	Distributed along termination resistors. Distribute evenly across domain.	16x 1 μF (0402) 4x 10 μF (0603)

Figure 3-1: DDR4 MD Strobe/Data Signal Topology



Figure 3-2: DDR4 MD CLK Signal Topology

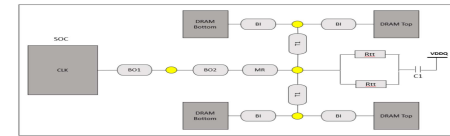


Figure 3-3: DDR4 MD CMD/CTRL Signal Topology

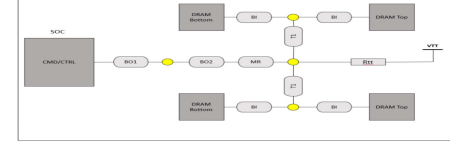


Figure 3-4: DDR4 MD ALERT Signal Topology

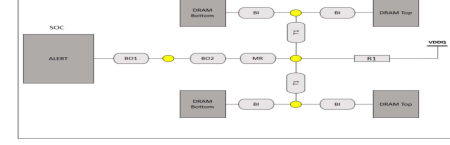
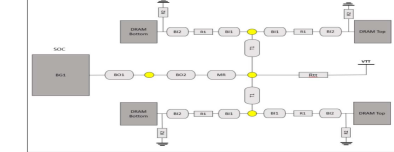
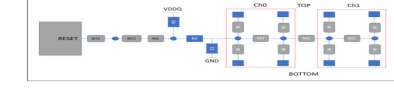


Figure 3-5: BG1 Topology for SDP-DDP Compatibility

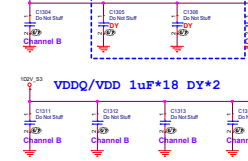


NOTE: For BG1 compatibility across SDP and DDP x16 devices:
• For SDP: R1 = Unstuffed, R2 = 0 Ohm
• For DDP: R1 = 0 Ohm, R2 = Unstuffed
• R12 < 2 mm, R1 + R2 < 12 mm
• R2 < 0.25 mm
• Choose resistors with very low ESL.

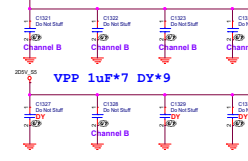
Figure 3-6: DDR4 MD Resets Signal Topology



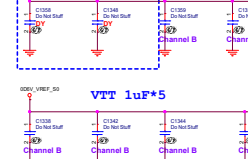
VDDQ/VDD 10uF*4 DY*2



VDDQ/VDD 1uF*18 DY*2



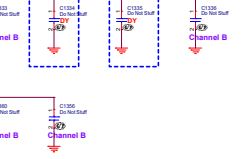
VPP 1uF*7 DY*9



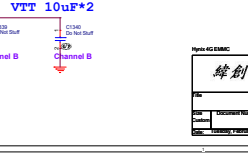
VTT 1uF*5



VPP 10uF*3 DY*1



VTT 10uF*2



Blanking

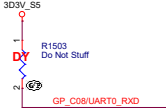
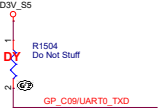

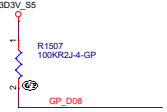
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Size <div>A4</div>	Document Number <div>Airking_JL</div>	Rev <div>-1</div>
Date: Tuesday, February 23, 2021		Sheet 14 of 106


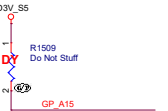




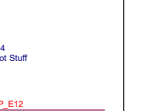
20 GP_C08(UART0_RXD) >>>
20 GP_C09(UART0_TXD) >>>
20 GP_C10 >>>
20 GP_D08 >>>
20 GP_D09 >>>
4 GP_A15 >>>
20 GP_E06 >>>
4 GP_E14 >>>
4.57 HDMI_SDA_CPU >>>
4 GP_E18 >>>
20 GP_E12 >>>
3 DBG_PMODE >>>
17 GP_DSW07 >>>

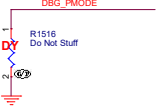


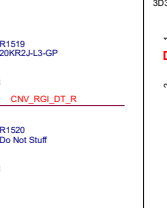
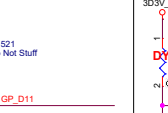
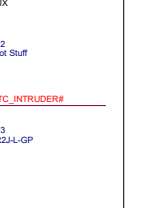
20 GP_D11 >>>

Description	Top Swap Override	No Reboot	TLS Confidentiality	eSPI Disable	Reserved	CPUNSSC Clock Frequency	Reserved
GPIO	GP_C01	GP_C02	GP_C08	GP_C09	GP_C10	GP_C13	GP_D08
Schematics							
High	Enable	Enable	Enable	Disable		19.2 MHz clock (derived from 38.4 MHz crystal)	
Low	Disable	Disable	Disable	Enable		38.4 MHz clock (direct from crystal)	
	internal pull-down 20 kohm ± 30%	internal pull-down 20 kohm ± 30%	internal pull-down 20 kohm ± 30%	internal pull-down 20 kohm ± 30%		internal pull-down 20 kohm ± 30%	

20 GP_E00 >>>
21 CNV_RGI_DT_R >>>

17 RTC_INTRUDER# >>>

Description	Reserved	Flash Descriptor Security Override	Reserved	BSSB LSX 0 pins VCC Configurati on	BSSB LSX 1 pins VCC Configurati on	BSSB LSX 2 pins VCC Configurati on	BSSB LSX 3 pins VCC Configurati on
GPIO	GP_D09	GP_A15	GP_E06	GP_E14	GP_E16	GP_E18	GP_E12
Schematics							
High		Disable		3.3V	3.3V	3.3V	3.3V
Low		Enable		1.8V	1.8V	1.8V	1.8V
		internal pull-down 20 kohm ± 30%		internal pull-down 20 kohm	internal pull-down 20 kohm	internal pull-down 20 kohm	internal pull-down 20 kohm

Description	RSVD	Reserved	Reserved	XTAL Frequency Selection	M.2 CNVi Mode Select	eSPI Flash Sharing Mode	SPI Voltage Configuration
GPIO	GP_D10	DBG_PMODE	GP_DSW07	GP_E00	GP_E22	GP_D11	INTRUDER#
Schematics							
High				24 MHz	Disable	(SAFS) enabled	SPI = 1.8V
Low				38.4 MHz / 19.2 MHz	Enable	(MAFS) enabled	SPI = 3.3V
	internal pull-down 20 kohm	internal pull-up 20 kohm ± 30%	internal pull-down 20 kohm ± 30%	internal pull-down 20 kohm ± 30%	internal pull-down 20 kohm ± 30%	internal pull-down 20 kohm ± 30%	

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61,89 WLAN_PCIE_RX_N
61,89 WLAN_PCIE_RX_P
61,89 WLAN_PCIE_TX_C_N
61,89 WLAN_PCIE_TX_C_P
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Document Number: 613095 Ver 0.9
220 nF nominal capacitors are recommended for Gen 3
100 nF nominal capacitors are recommended for Gen 2

73	USB3_USB30_RX_N0	↔
73	USB3_USB30_RX_P0	↔
73	USB3_USB30_TX_N0	↔
73	USB3_USB30_TX_P0	↔
73	USB3_USB30_RX_N1	↔
73	USB3_USB30_RX_P1	↔
73	USB3_USB30_TX_N1	↔
73	USB3_USB30_TX_P1	↔
73	USB3_USB20_N	↔
73	USB3_USB20_P	↔

63	SSD1_PCIE_RX_N0	
63	SSD1_PCIE_RX_P0	
63	SSD1_PCIE_TX_N0	
63	SSD1_PCIE_TX_P0	
63	SSD1_PCIE_RX_N1	
63	SSD1_PCIE_RX_P1	
63	SSD1_PCIE_TX_N1	
63	SSD1_PCIE_TX_P1	
63	SSD1_PCIE_RX_N2	
63	SSD1_PCIE_RX_P2	
63	SSD1_PCIE_TX_N2	
63	SSD1_PCIE_TX_P2	
63	SSD1_PCIE_RX_N3	
63	SSD1_PCIE_RX_P3	
63	SSD1_PCIE_TX_N3	
63	SSD1_PCIE_TX_P3	
63	SSD1_SATA_TX_P0	
63	SSD1_SATA_TX_N0	
63	SSD1_SATA_RX_P0	
63	SSD1_SATA_RX_N0	

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35 USB1_USB30_RX_N
35 USB1_USB30_RX_P
35 USB1_USB30_TX_N
35 USB1_USB30_TX_P

36 Charger_USB20_N
36 Charger_USB20_P

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66 USB2_USB30_RX_N
66 USB2_USB30_RX_P
66 USB2_USB30_TX_N
66 USB2_USB30_TX_P

66,89 USB2_USB20_P
66,89 USB2_USB20_N

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55 CCD_USB20_N
55 CCD_USB20_P

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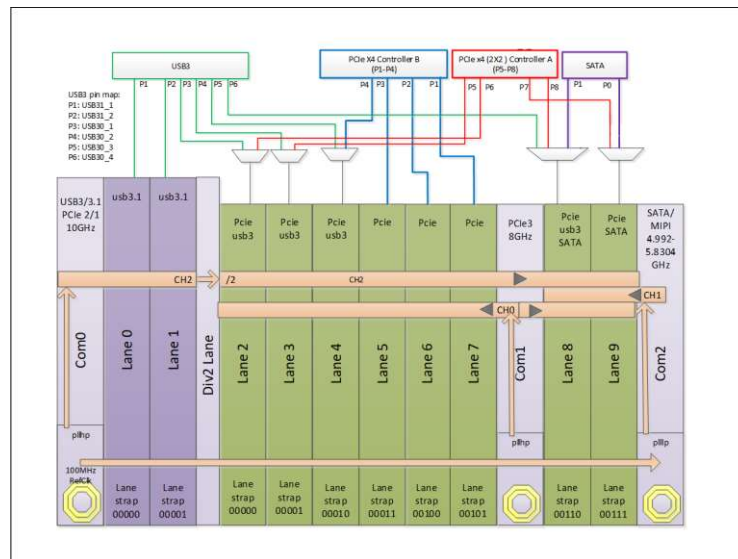
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61.89 BT_USB20_P



- ### Example Internal USB Port Assignments in PCH

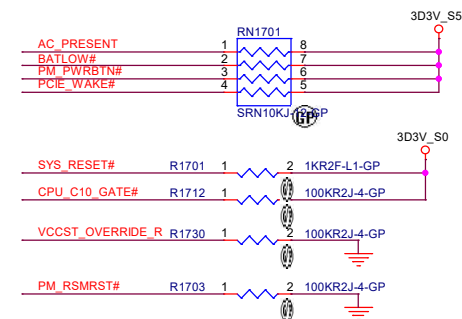
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USB Port Number (Zero-based) (When starting with "1", e.g., BIOS)	Port 7 Port 8

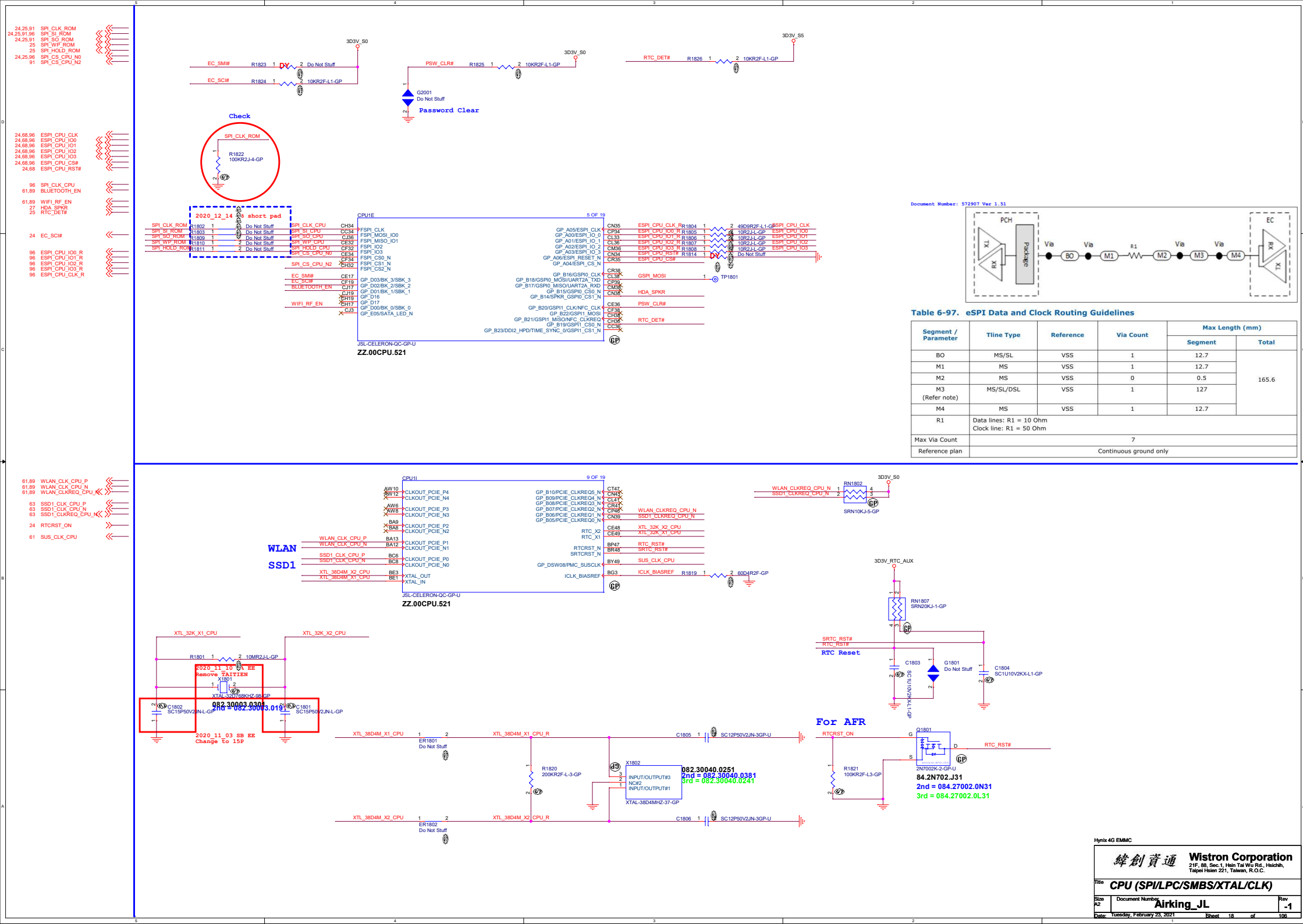


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61 CNV_WT_DN0
61 CNV_WT_DP0
61 CNV_WT_DN1
61 CNV_WT_DP1
61 CNV_WT_CLKN
61 CNV_WT_CLKP

61 CNV_WR_DN0
61 CNV_WR_DP0
61 CNV_WR_DN1
61 CNV_WR_DP1
61 CNV_WR_CLKN
61 CNV_WR_CLKP

61 CNV_BRI_RSP
61 CNV_RGI_DT
61 CNV_BRI_DT
61 CNV_RGI_RSP

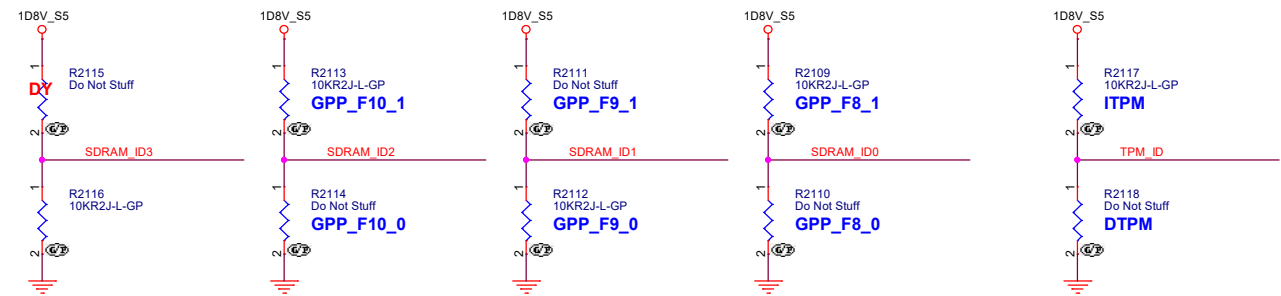
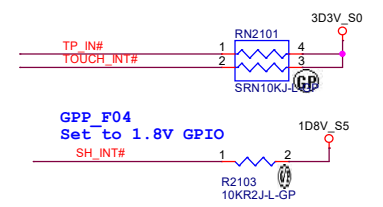
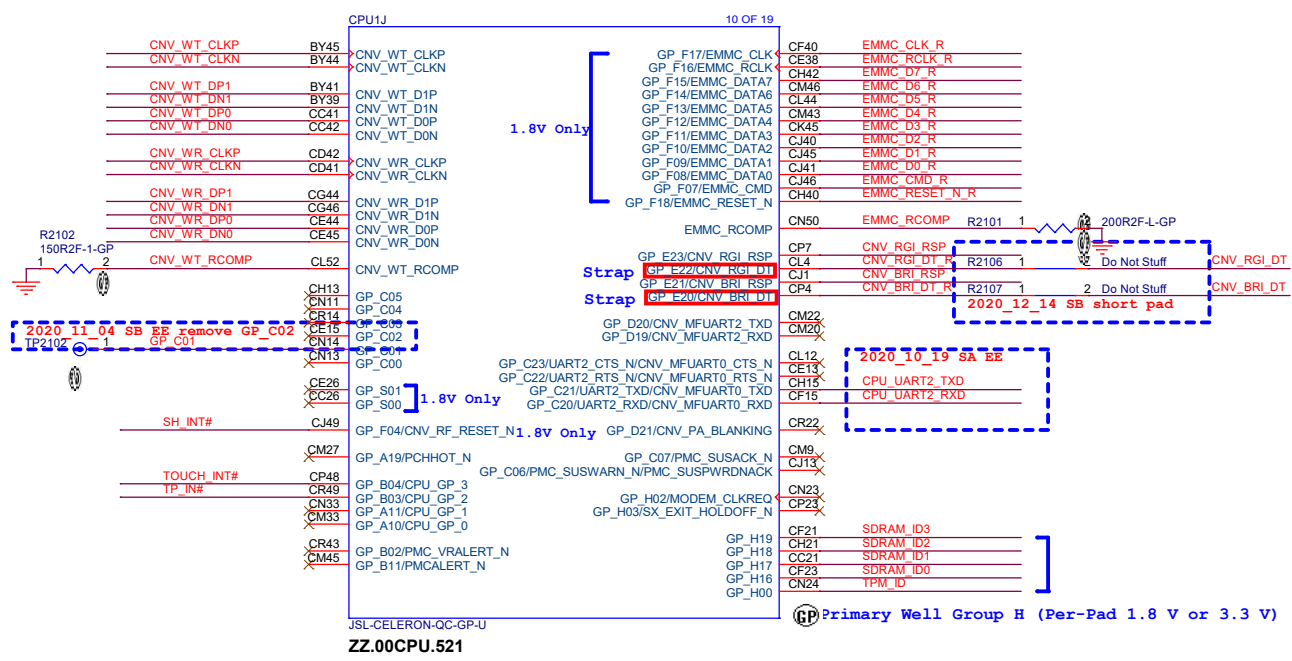
15 CNV_RGI_DT_R

65 TP_IN#

24 SH_INT#
55 TOUCH_INT#

63 EMMC_RCLK_R
63.96 EMMC_CLK_R
63.96 EMMC_D7_R
63 EMMC_D6_R
63 EMMC_D5_R
63 EMMC_D4_R
63 EMMC_D3_R
63 EMMC_D2_R
63 EMMC_D1_R
63.96 EMMC_D0_R
63.96 EMMC_CMD_R
63 EMMC_RESET_N_R

68 CPU_UART2_RXD
68 CPU_UART2_TXD



Vendor	SDRAM_ID3	SDRAM_ID2	SDRAM_ID1	SDRAM_ID0	WISTRON PN	Vendor PN	Capacity	Channel	DDP/SDP
MICRON	0	0	0	0	KN.8GB04.050	MT40A512M16LY-062E	8Gb	A+B	SDP
	0	0	0	1					
HYNIX	0	0	1	0	KN.8GB0G.071	H5AN8G6NDJR-XNC	8Gb	A+B	SDP
MICRON	0	0	1	1	KN.8GB04.050	MT40A512M16LY-062E	4Gb	A	SDP
	0	1	0	0					
HYNIX	0	1	0	1	KN.8GB0G.071	H5AN8G6NDJR-XNC	4Gb	A	SDP

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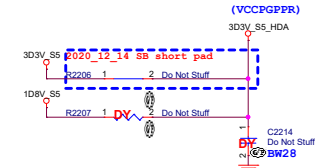
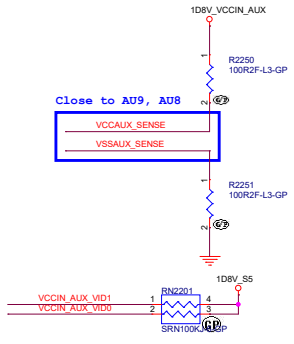
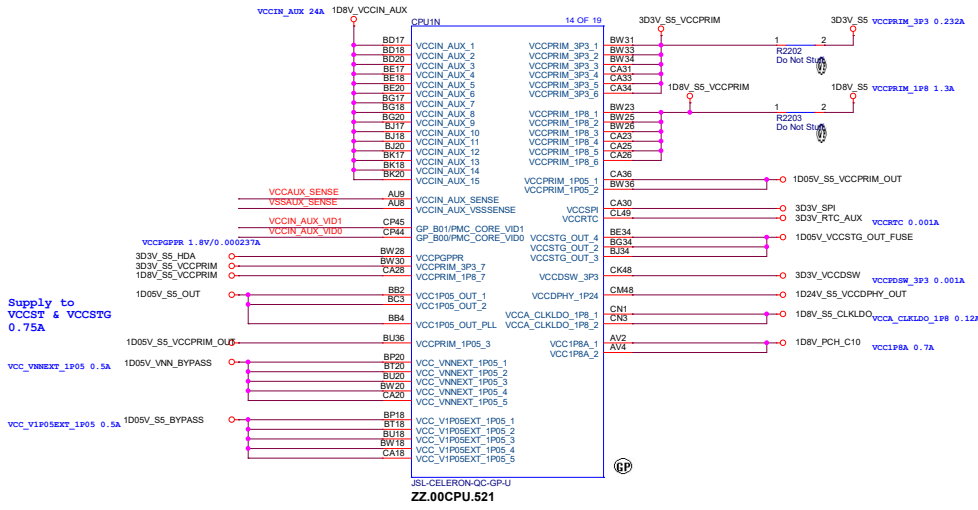
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Title CPU (CS/EMMC/CNVi)

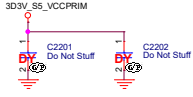
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50 VCCAUX_SENSE
50 VSSAUX_SENSE
40.50 VCCIN_AUX_VID1
40.50 VCCIN_AUX_VID0



Domain	Primary Side Cap	Secondary Side Cap
VCCPGPPR	N/A	N/A



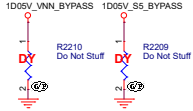
Domain	Primary Side Cap	Secondary Side Cap
VCCPRIM_3P3	Place holder: 1 x 0402 1 x 0402	None



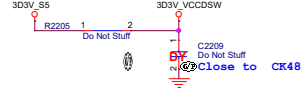
Domain	Primary Side Cap	Secondary Side Cap
VCCPRIM_1P8	Place holder: 1 x 0402	None



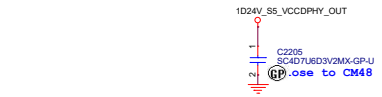
Domain	Primary Side Cap	Secondary Side Cap
VCCSPI	N/A	N/A



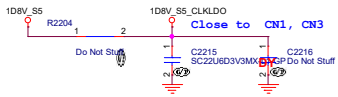
Domain	Top Side Cap	Backside Side Cap
VCCRTC	1 x 0402_1uF 1 x 0402_0.1uF	NA



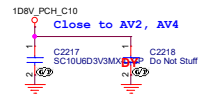
Domain	Primary Side Cap	Secondary Side Cap
VCCDSW_3P3	Place holder: 1 x 0402	NA



Domain	Primary Side Cap	Secondary Side Cap
VCCDPHY_1P24 (do not connect to power)	1 x 0402_4.7uF	NA



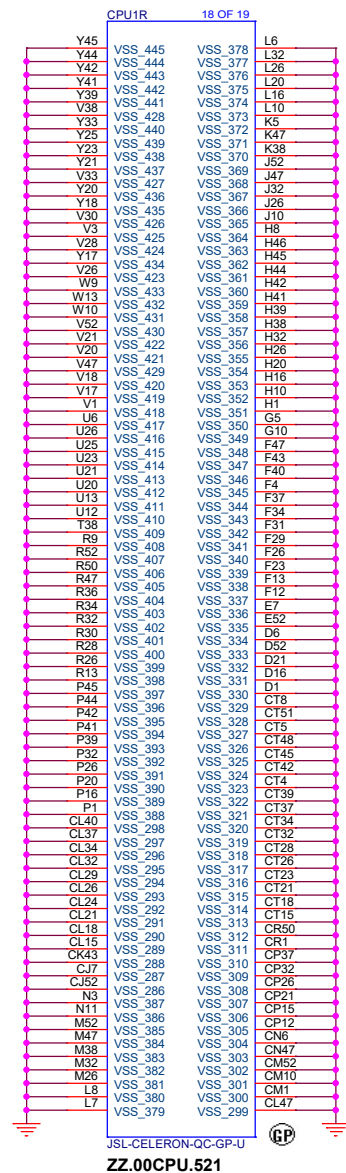
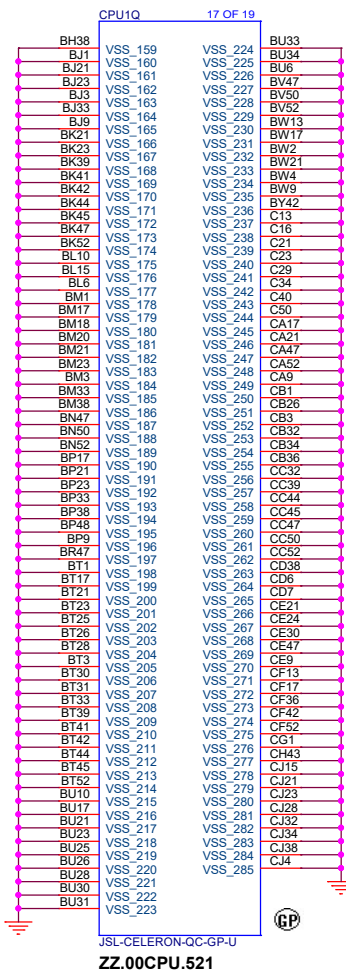
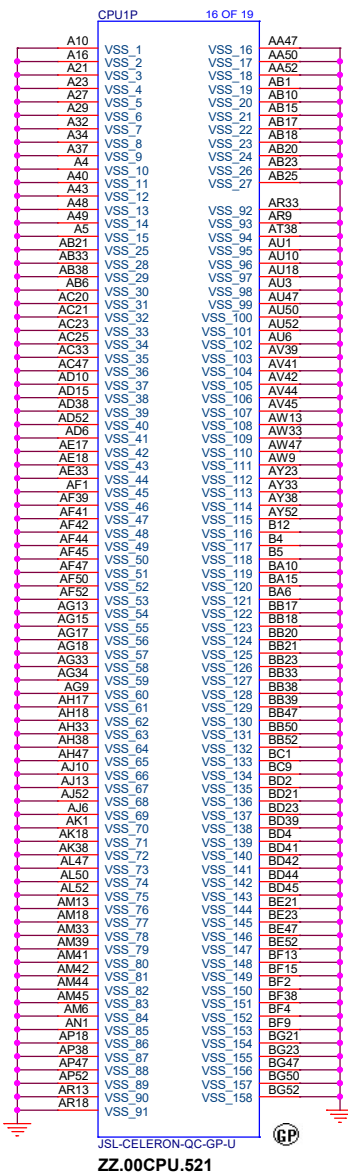
Domain	Primary Side	Secondary Side
VCCA_CLKLDO_1P8	LC filter: L = 0.68uH (2mm x 2mm) R = 100mOhm; Min current rating = 150mA The inductor need to meet this RL. C = 47uF (0603/0805)	None



Domain	Primary Side Cap	Secondary Side Cap
VCC1P8A	1 x 0402_10uF	None



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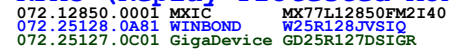


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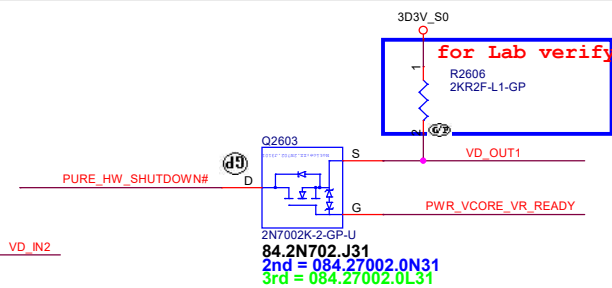
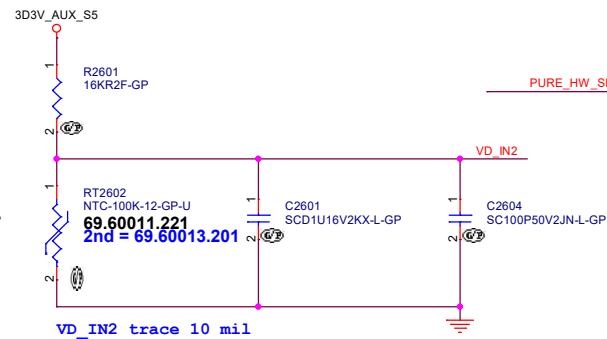
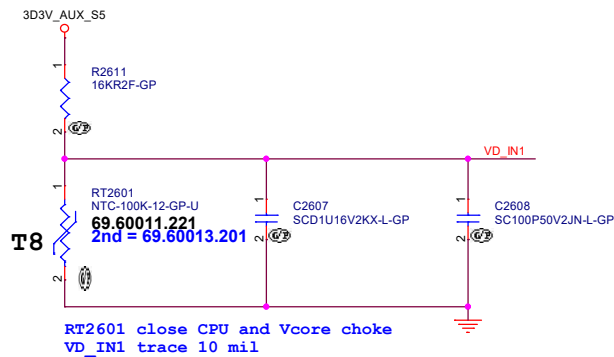
SPI Flash ROM (16M Byte)



RTC BATTERY (90mm)
1st= 23.21212.091 KTS
2nd= 023.22032.0901 TIANQIU
3rd= 23.21221.091 JHT

SSID = Thermal

24 VD_IN1
24 VD_IN2
24.40 PURE_HW_SHUTDOWN#
24 VD_OUT1
40.46 PWR_VCORE_VR_READY



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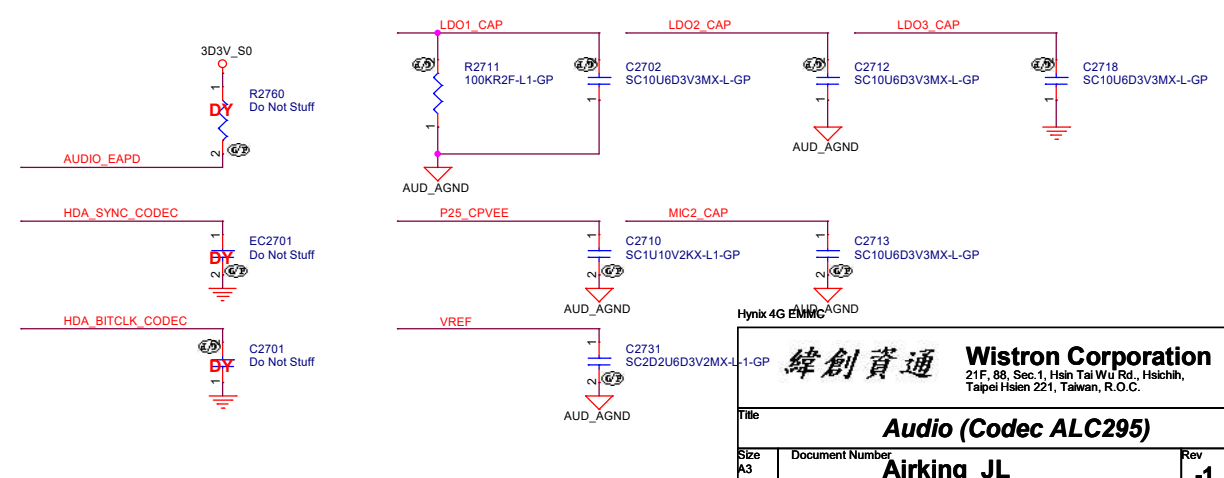
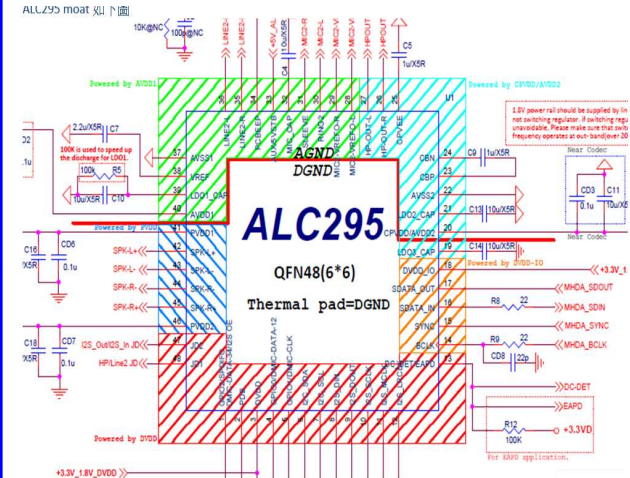
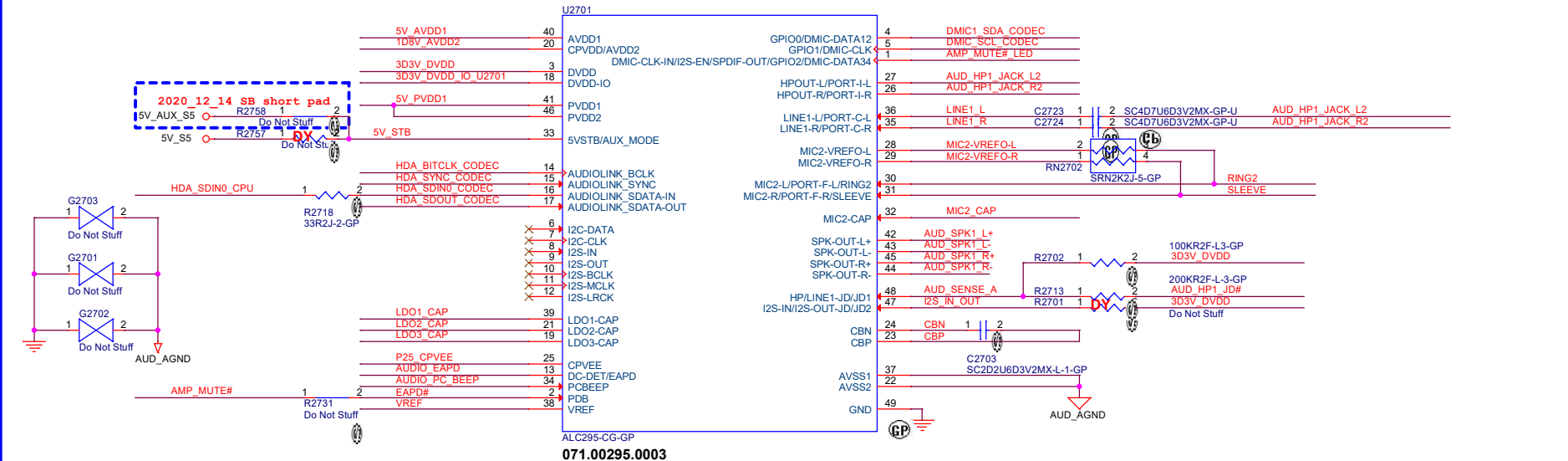
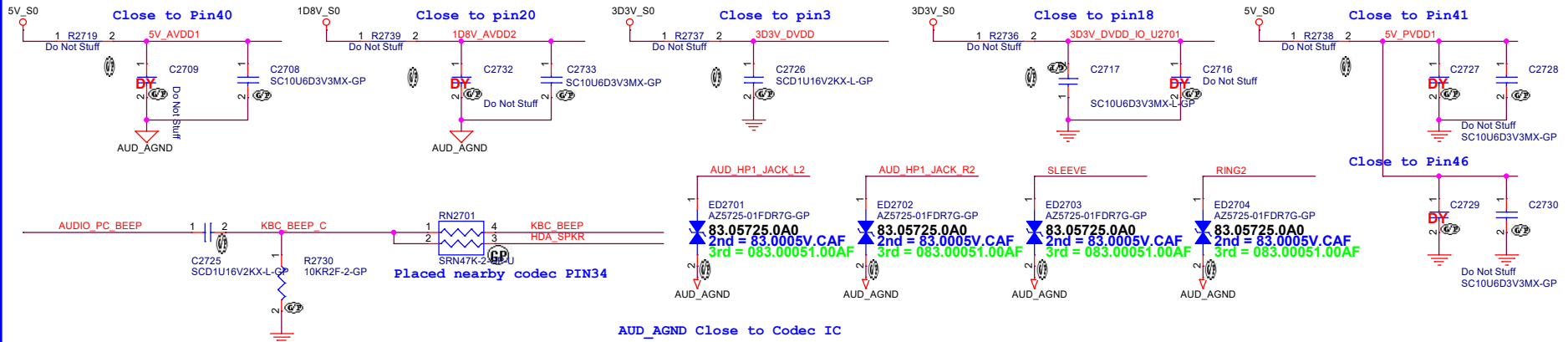
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SSID = AUDIO

- 19,96 HDA_SYNC_CODEC
19,96 HDA_BITCLK_CODEC
19,96 HDA_SDOUT_CODEC
19,96 HDA_SDIN0_CPU
- 24 KBC_BEEP
18 HDA_SPKR
24 AMP_MUTE#
- 66,89 AUD_HP1_JACK_L2
66,89 AUD_HP1_JACK_R2
- 66,89 RING2
66 SLEEVE
66 AUD_HP1_JD#
- 29 AUD_SPK1_L+
29 AUD_SPK1_L-
29 AUD_SPK1_R+
29 AUD_SPK1_R-
- 55 DMIC1_SDA_CODEC
55 DMIC_SCL_CODEC
- 65 AMP_MUTE#_LED



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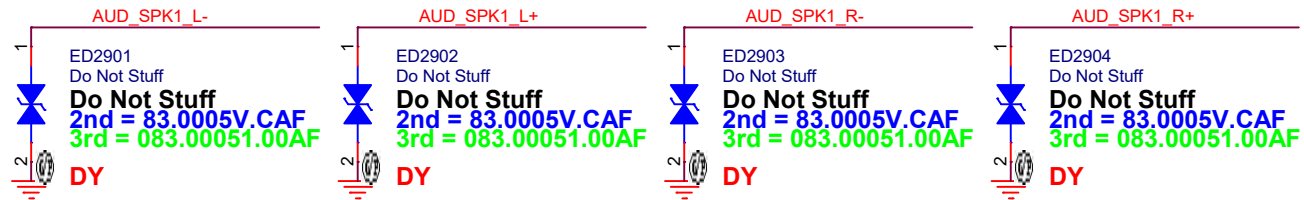
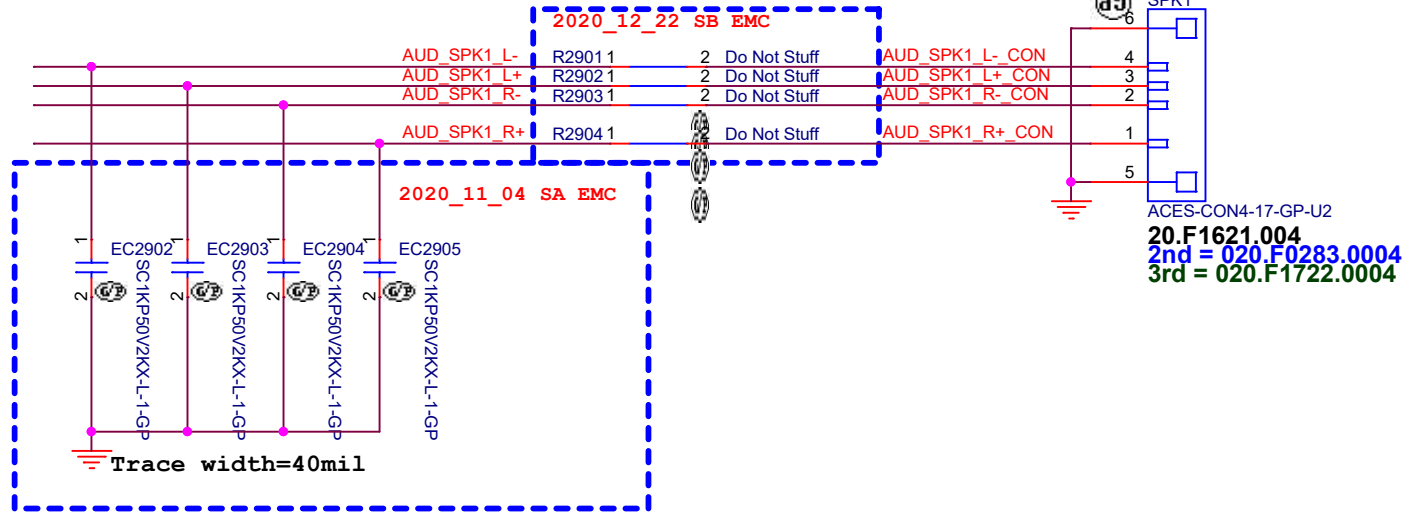
Title			Audio (RSVD)		
Size	Document Number				Rev
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Date:	Tuesday, February 23, 2021		Sheet	28	of 106

27 AUD_SPK1_L-
27 AUD_SPK1_L+
27 AUD_SPK1_R-
27 AUD_SPK1_R+

89 AUD_SPK1_R+_CON
89 AUD_SPK1_R-_CON
89 AUD_SPK1_L+_CON
89 AUD_SPK1_L-_CON

SSID = AUDIO

Speaker



ALC295:

		DVDD (1.8V/3.3V)	DVDD-IO (1.5V/3.3V)	AVDD1 (5V)	AVDD2+CPVDD (1.8V)	PVDD1/2 (5V)
		(mA)	(mA)	(mA)	(mA)	(mA)
1	DVDD=1.8V, DVDD-IO=1.5V	10	5	50	200	1500
2	DVDD=3.3V, DVDD-IO=3.3V	10	5	50	200	1500

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A4	Airking_JL		-1	
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Title <div>Audio (RSVD)</div>		
Size <div>A4</div>	Document Number <div>Airking_JL</div>	Rev <div>-1</div>
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Title <div>LAN (RSVD)</div>		
Size <div>A4</div>	Document Number <div>Airking_JL</div>	Rev <div>-1</div>
Date: Tuesday, February 23, 2021		Sheet 31 of 106

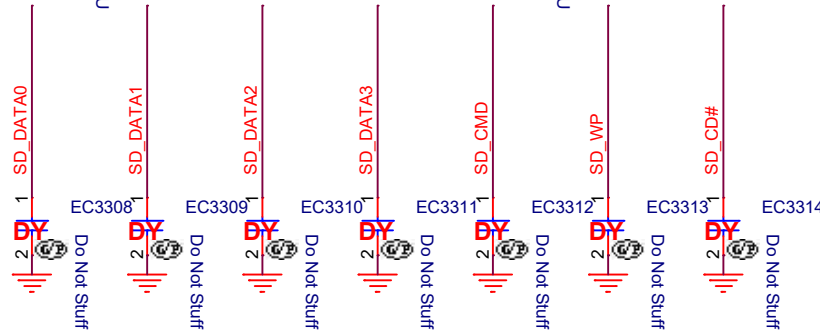
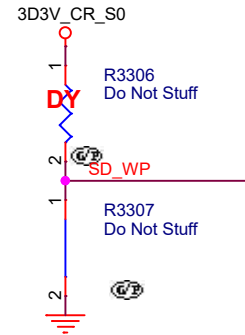
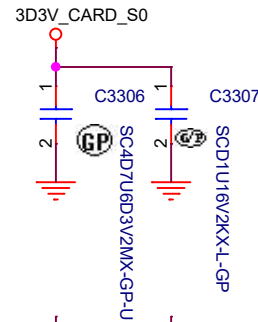
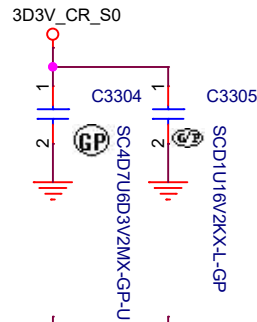
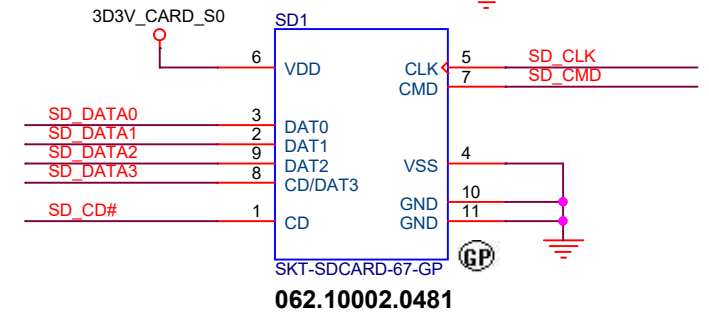
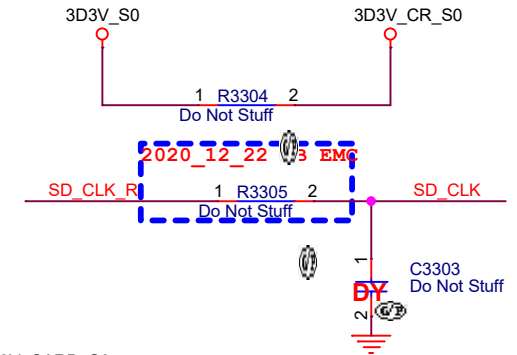
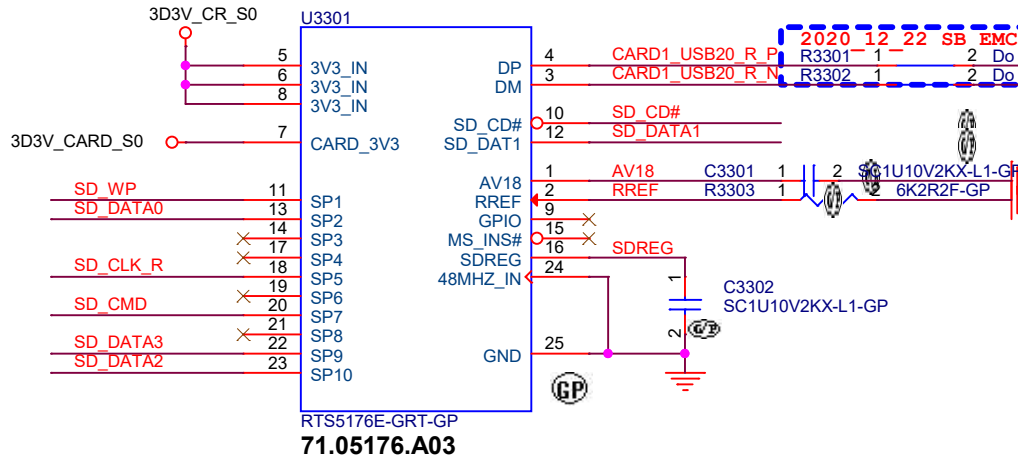
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Title <div>LAN (RSVD)</div>		
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16 CARD1_USB20_P
16 CARD1_USB20_N
89 CARD1_USB20_R_P
89 CARD1_USB20_R_N



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Title		
CARDREADER (SD Conn)		
Size A4	Document Number Airking_JL	Rev -1
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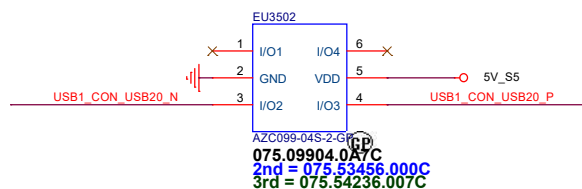
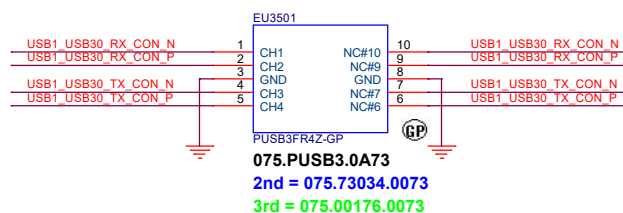
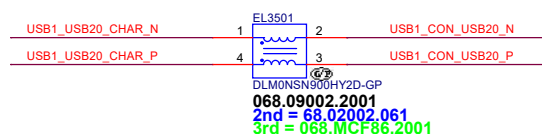
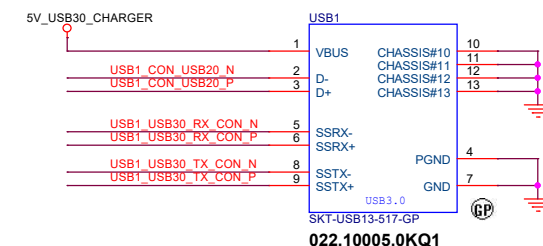
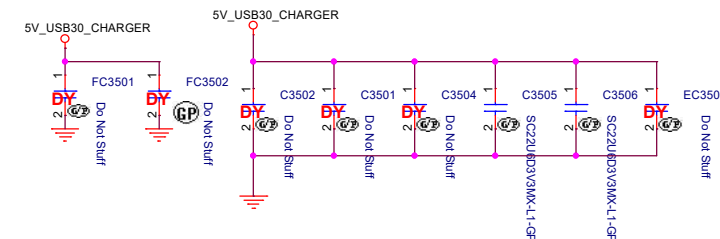
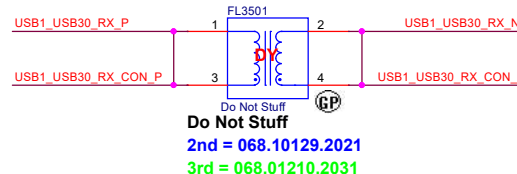
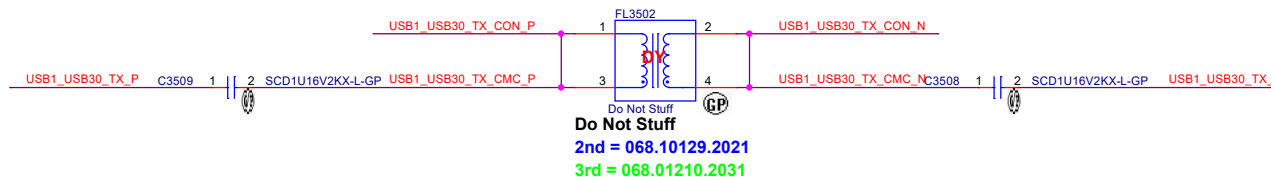
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Title <div>USB (RSVD)</div>		
Size <div>A4</div>	Document Number <div>Airking_JL</div>	Rev <div>-1</div>
Date: Tuesday, February 23, 2021		Sheet 34 of 106

36 USB1_USB20_CHAR_N
36 USB1_USB20_CHAR_P
16 USB1_USB30_RX_N
16 USB1_USB30_RX_P
16 USB1_USB30_TX_N
16 USB1_USB30_TX_P
89 USB1_CON_USB20_N
89 USB1_CON_USB20_P



USB 3.0 Connector Pin definition

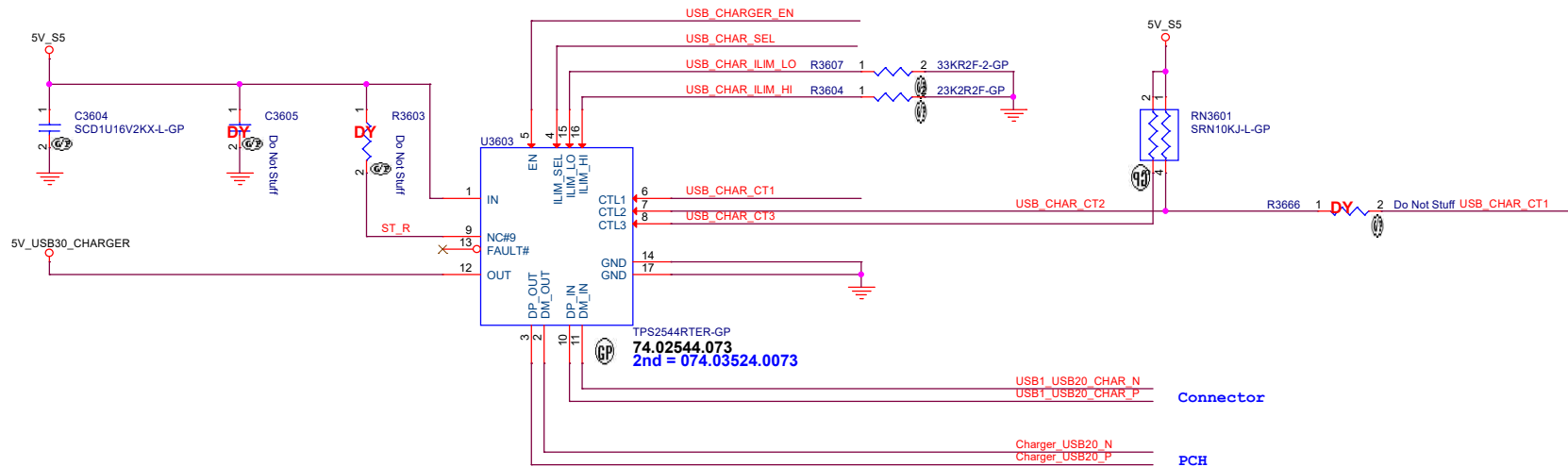
1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	StdA_SSRX- SuperSpeed RX
6	StdA_SSRX+
7	GND
8	StdA_SSTX- SuperSpeed TX
9	StdA_SSTX+

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Title	USB (USB3.0 CONN)		
Size	Document Number	A3	Rev
	Airking_JL		-1
Date:	Tuesday, February 23, 2021	Sheet	35 of 106

24 USB_CHARGER_EN >>>
 24 USB_CHAR_SEL >>>
 24 USB_CHAR_CT1 >>>
PCH
 16 Charger_USB20_N <<<
 16 Charger_USB20_P <<<
Connector
 35 USB1_USB20_CHAR_N <<<
 35 USB1_USB20_CHAR_P <<<



CTL1	CTL2	CTL3	ILIM_SEL	Mode	Current Limit Setting	Comment
0	0	0	0	Discharge	NA	OUT held low
0	0	0	1	Discharge	NA	Data Lines
0	0	1	0	DCP_Auto	ILIM_HI	Disconnected
0	1	0	0	SDP1	ILIM_LO	Data Lines connected
0	1	0	1		ILIM_HI	
1	0	0	0	DCP Forced Shorted	ILIM_LO	Device Forced to stay in DCP BC 1.2 charging mode
1	0	0	1		ILIM_HI	
1	0	1	0	DCP / Divider1	ILIM_LO	Device Forced to stay in DCP Divider 1 Charging Mode
1	0	1	1		ILIM_HI	
1	1	0	0	SDP1	ILIM_LO	Data Lines
1	1	0	1	SDP1	ILIM_HI	Connected
1	1	1	0	SDP2 ⁽¹⁾	ILIM_LO	Connected
1	1	1	1	CDP ⁽¹⁾	ILIM_HI	Data Lines Connected

S5 (at low battery and non support charger)

S3 and S5 state

S0 and S3 (at low battery and non support charger)

S0 state

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Title			USB (USB Charger)	
Size A3	Document Number	Airking_JL		Rev -1
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Title			USB (RSVD)		
Size	Document Number				Rev
A4	Airking_JL				-1
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Title			USB (RSVD)		
Size	Document Number				Rev
A4	Airking_JL				-1
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TitleSequence (RSVD)		
SizeA4	Document NumberAirking_JL	Rev-1
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TitleSequence (RSVD)		
SizeA4	Document NumberAirking_JL	Rev-1
Date: Tuesday, February 23, 2021	Sheet 41 of	106

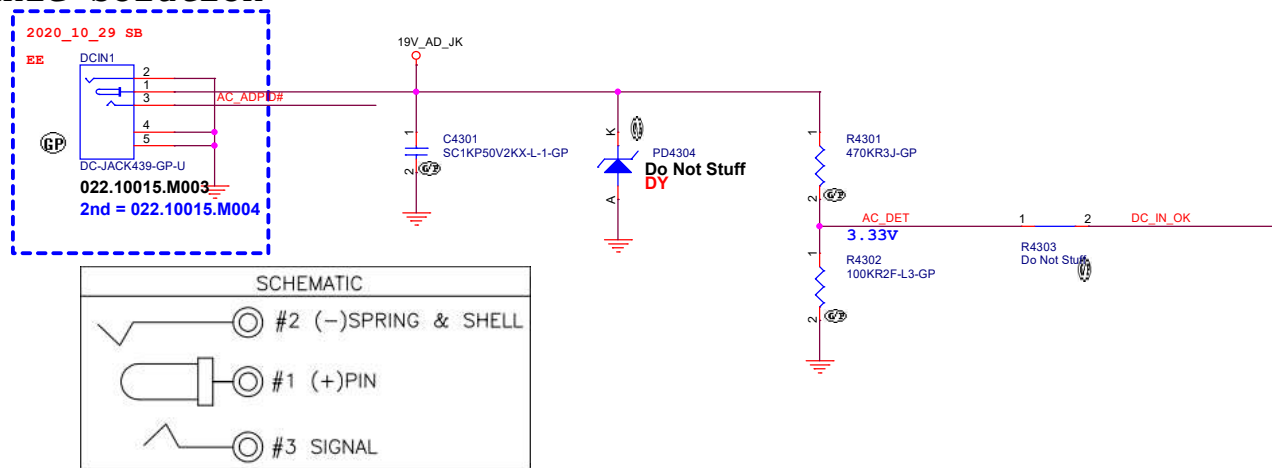
5	4	3	2	1
D				
C				
B				
A				

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Title			
INT IO (TYPEC DC-DC)			
Size	Document Number		Rev
A3	Airing_JL		-1
Date:	Tuesday, February 23, 2021		Sheet 42 of 106

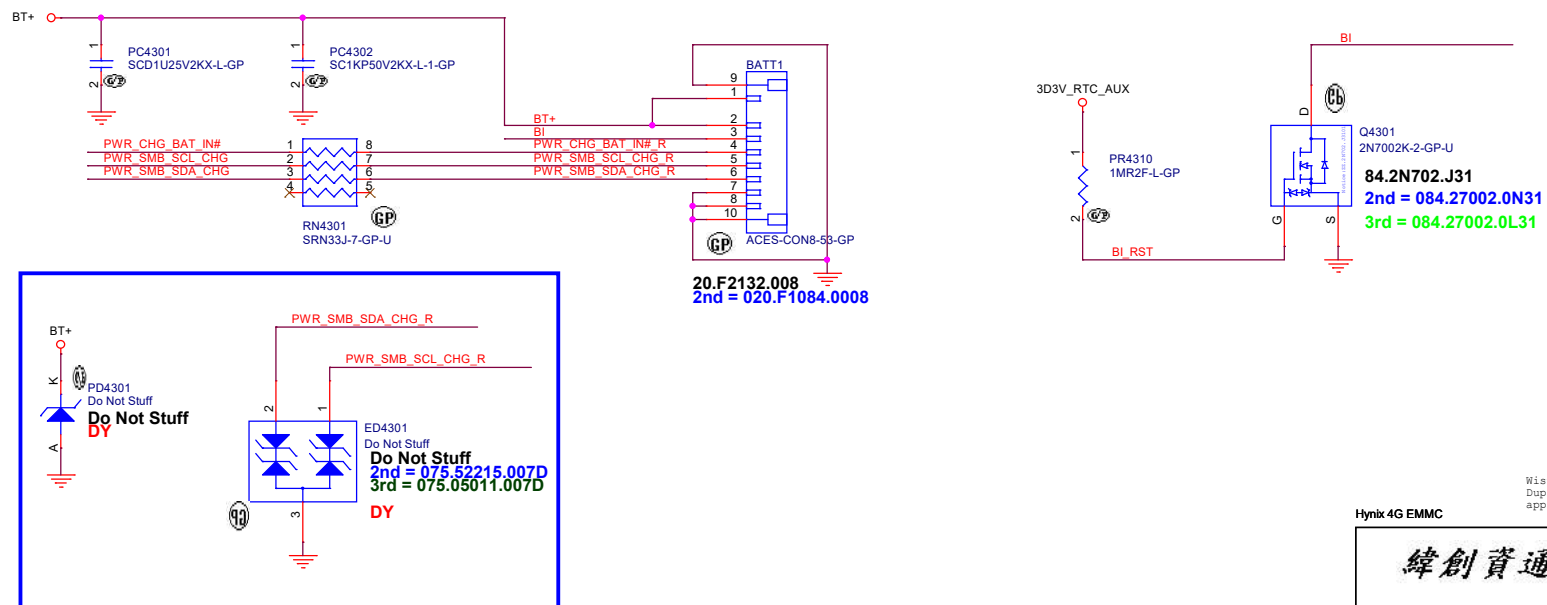
Annie Solution

44 AC_ADPI#
24 DC_IN_OK



Battery Connector

24,44,96 PWR_SMB_SCL_CHG
24,44,96 PWR_SMB_SDA_CHG
24,44 PWR_CHG_BAT_IN#
64,89 BI_RST
89 PWR_CHG_BAT_IN#_R
89,96 PWR_SMB_SCL_CHG_R
89,96 PWR_SMB_SDA_CHG_R
89 BI



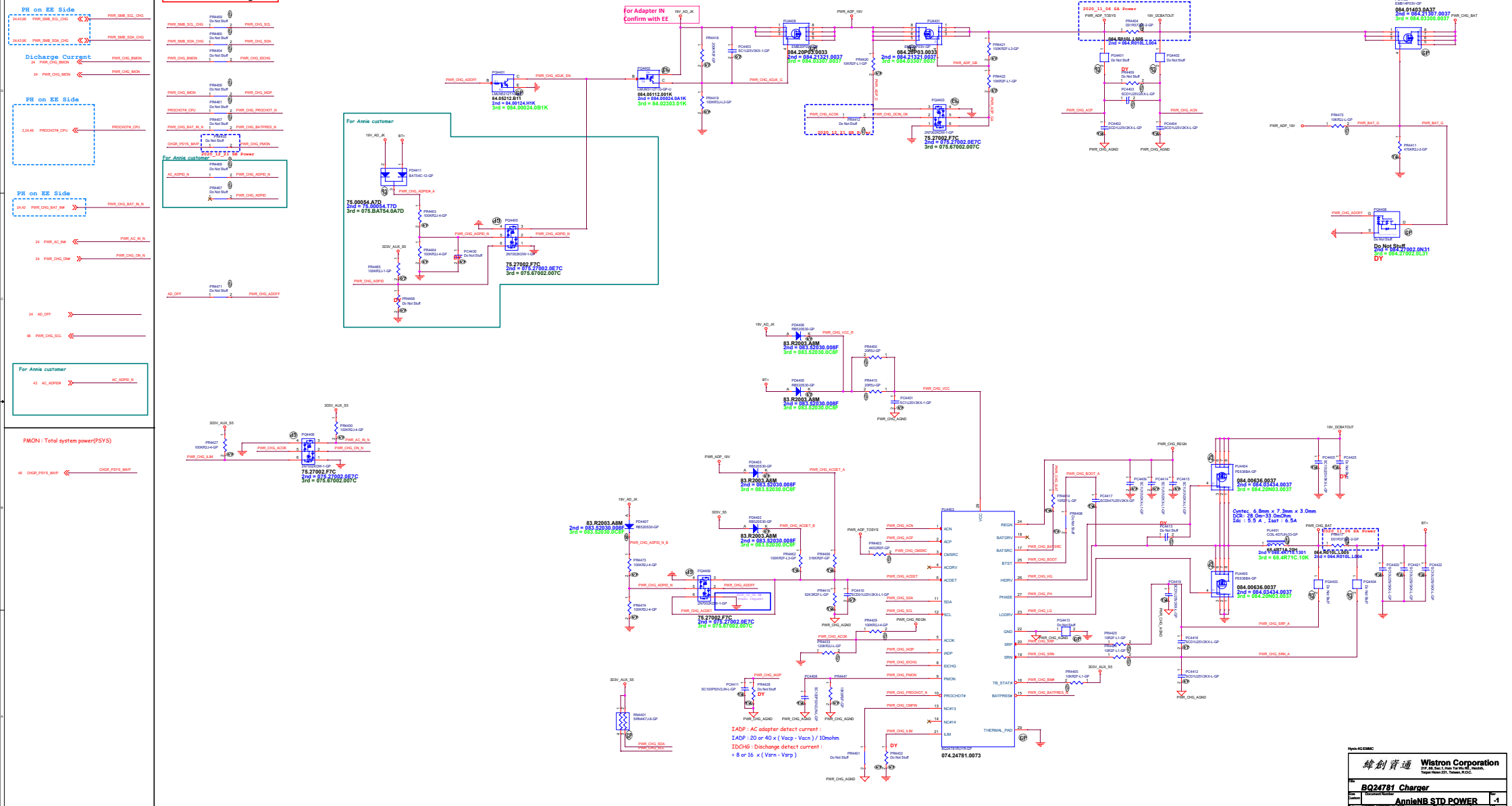
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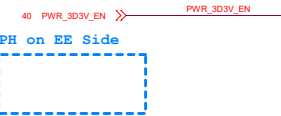
緯創資通 Wistron Corporation
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Title		
INT IO (DC/BATT Conn)		
Size	Document Number	Rev
A3	Airking_JL	-1
Date:	Tuesday, February 23, 2021	Sheet 43 of 106

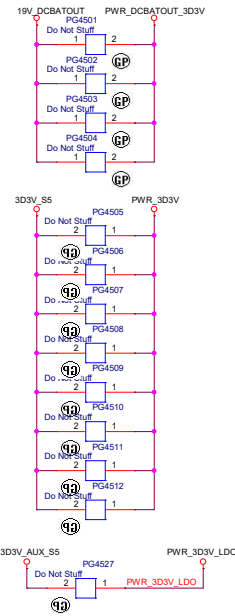
SSID = Charger



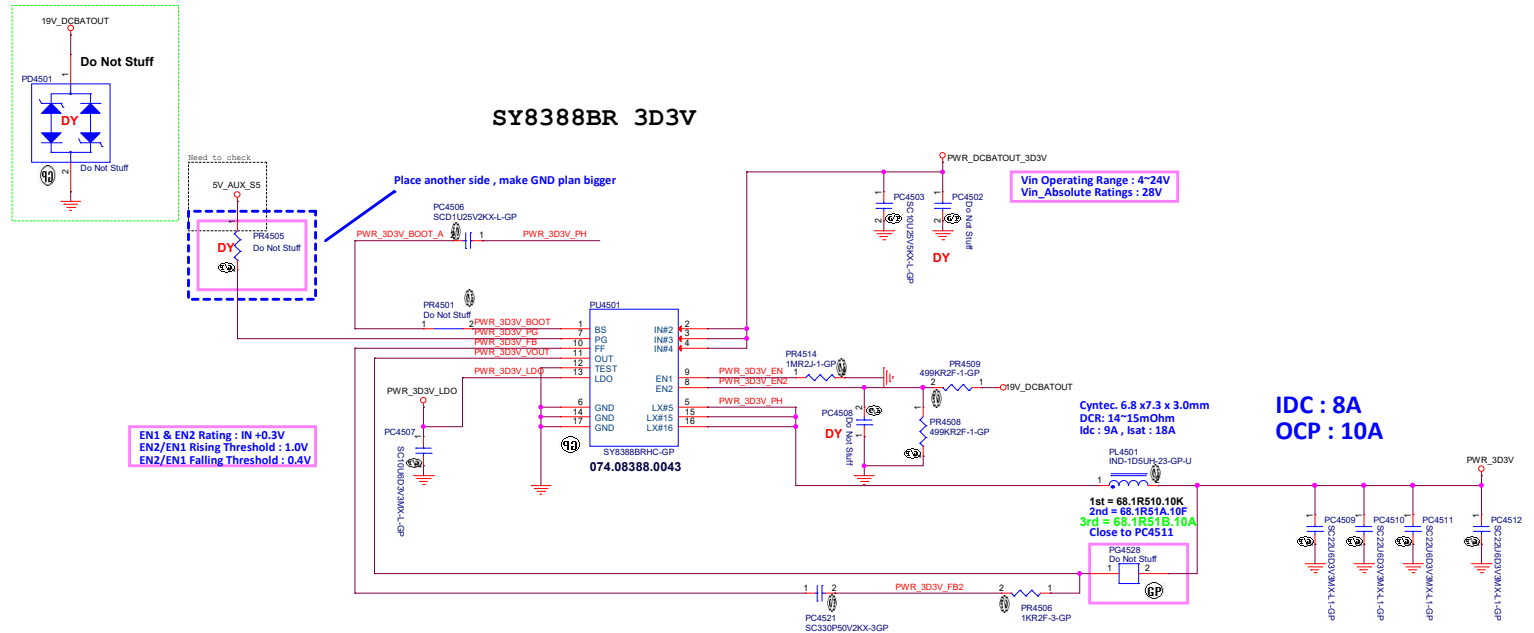
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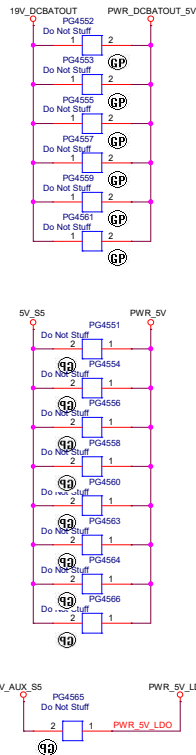
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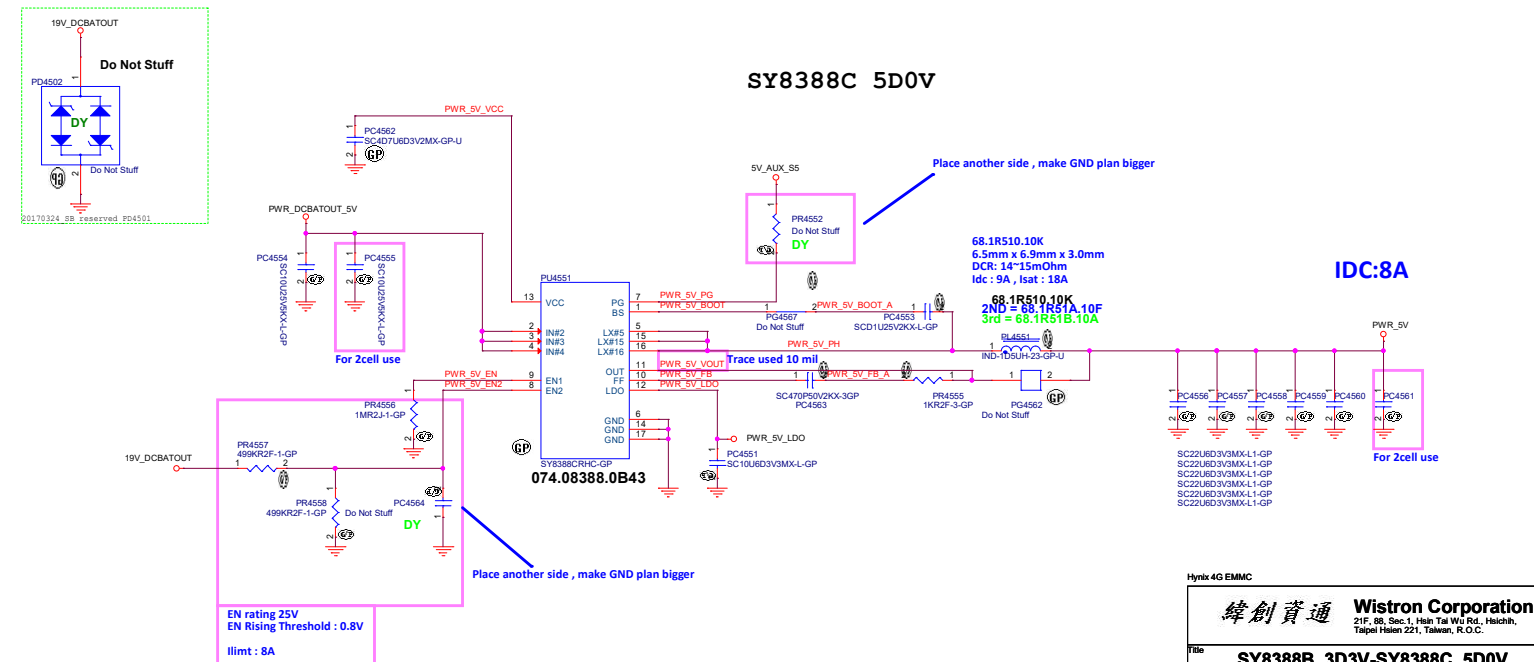
SY8388BR 3D3V



24 PWR_5V_EN >> PWR_5V_EN



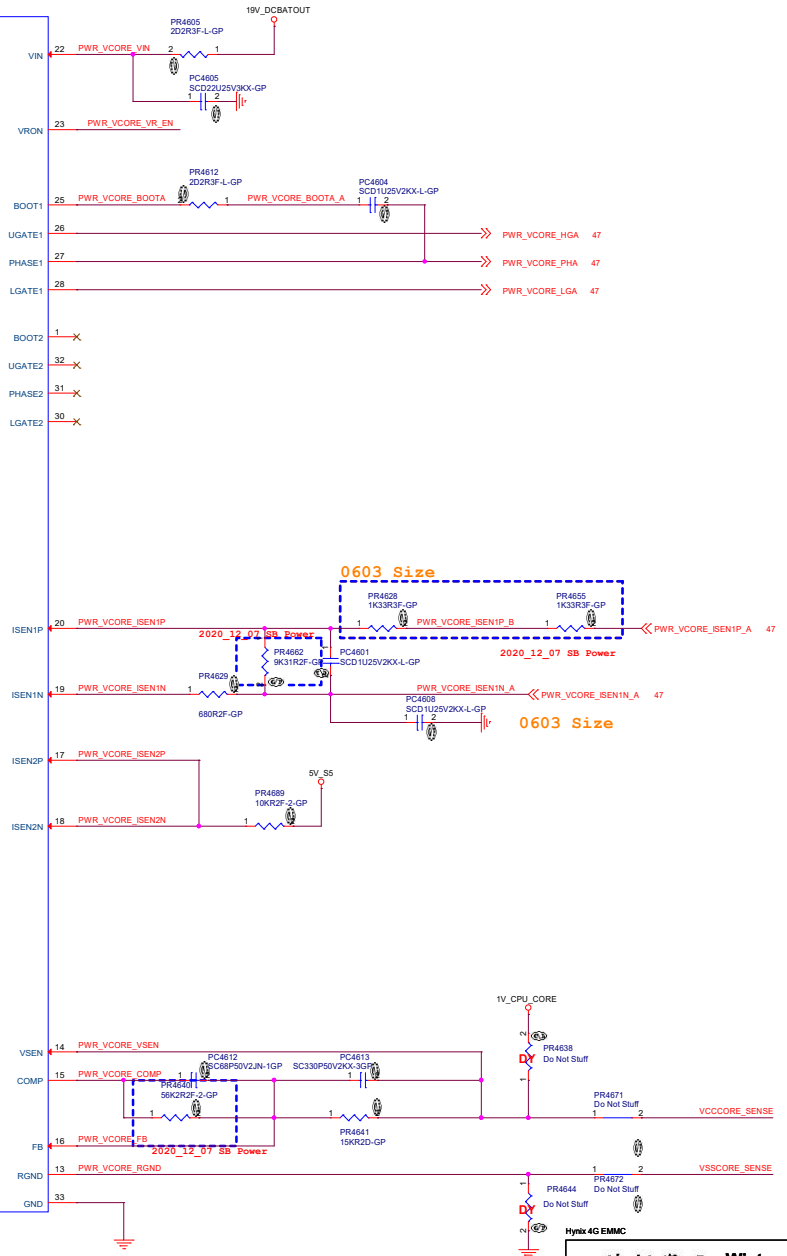
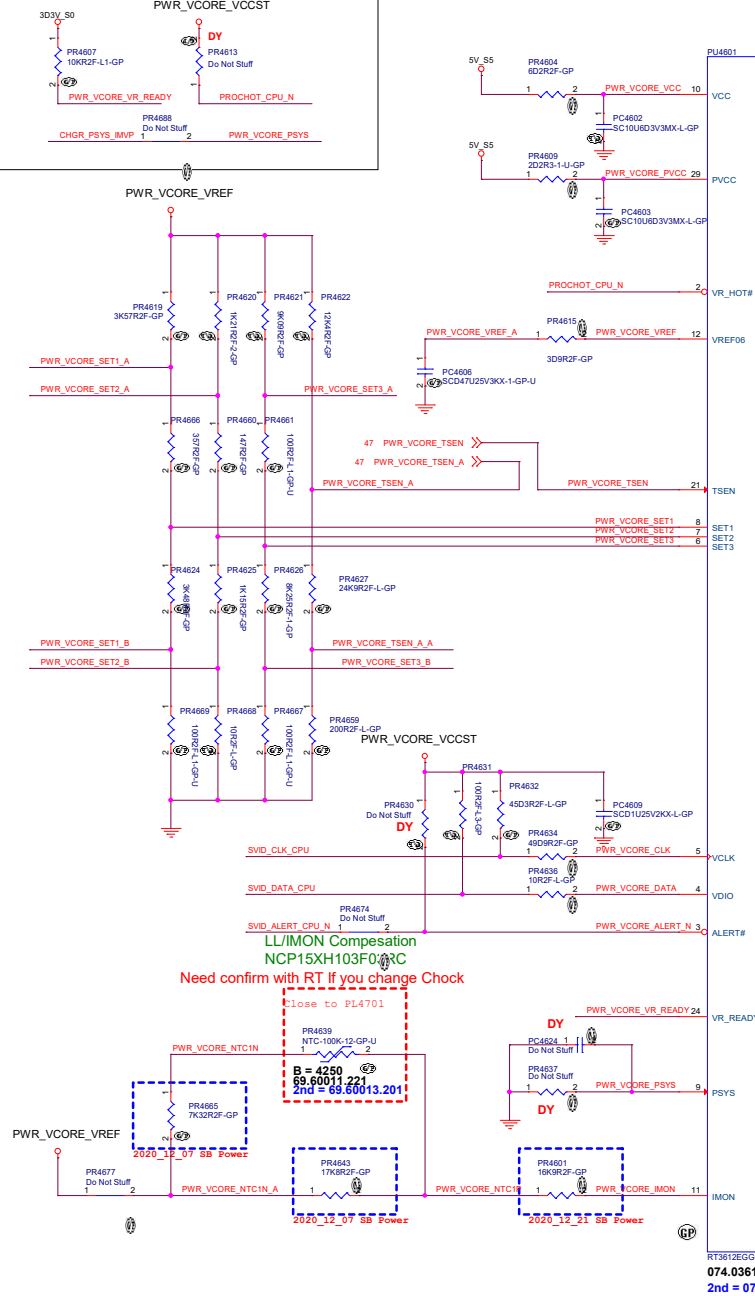
SY8388C 5D0V



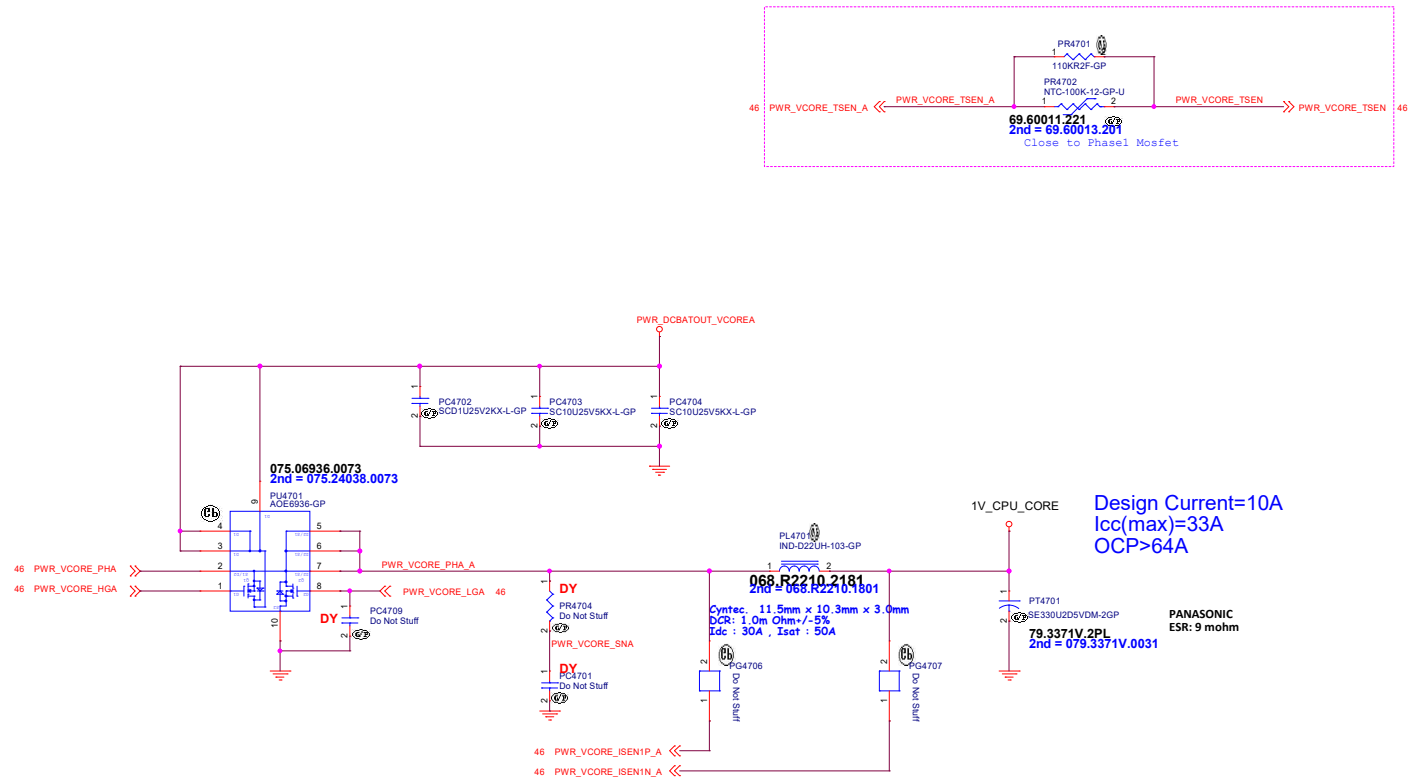
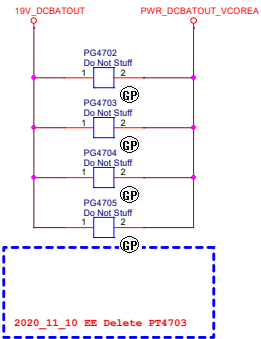
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File	SY8388B_3D3V-SY8388C_5D0V		
Size	Document Number		Rev
Custom	AnnieNB STD POWER		-1
Product: Laptop		Sheet: 45 of 100	

Reserve for Power test



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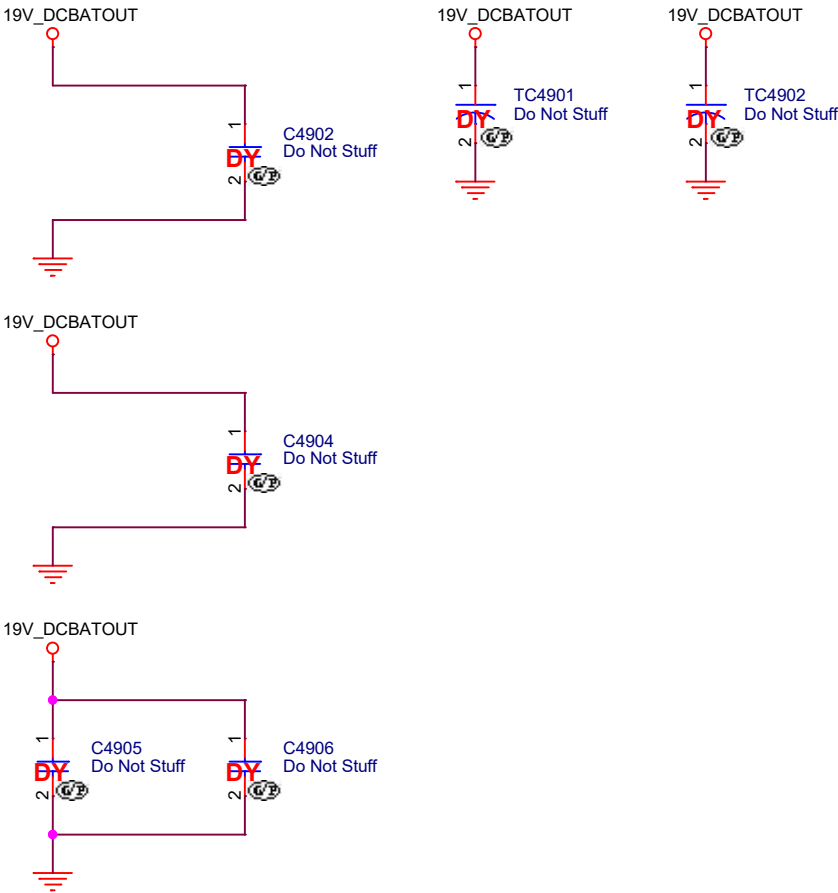
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Low Noise MLCC

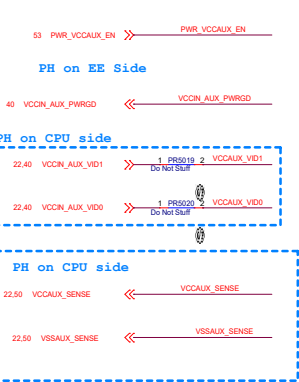


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Title			
POWER (EE Acoustic Noise)			
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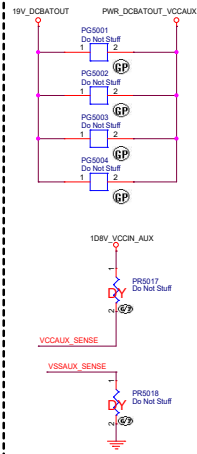


TABLE: MP2941 VID control Bit logics

VID1	VID0	VOUT(V)
0	0	0
0	1	1.1
1	0	1.65
1	1	1.8

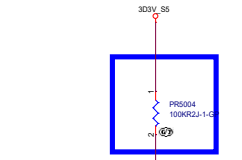


TABLE: MP2941 FS Selection

RMode	Fs
0	500kHz
90.9K	700kHz
150K	1000kHz
>230K or float	1200kHz

TABLE: MP2941 CLM/Phase Selection

RCLM	CLM
0	7A
90.9K	10A
150K	13A
>230K or float	16A

TABLE: MP2941 Mode Selection

RMode	Interleaving	VID Down
0	N	Slew down
90.9K	Y	Slew down
150K	Y	Decay
>230K or float	N	Decay

LOGIC

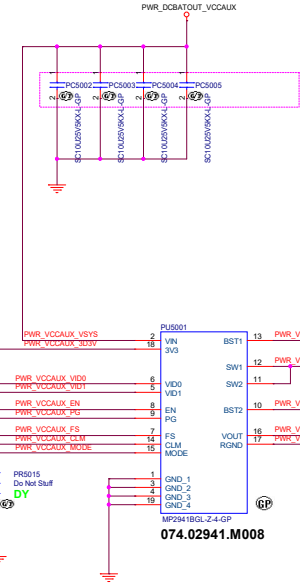
LOGIC

LOGIC

LOGIC

TABLE : MP2941

Item	R0 sample	R1 sample
VOUT	1.65V fixed	Defined by VCCPCHCORE_VID1/VID0
RMode	0 ohm	Float
RFS	Float	Float or 150K
1Kohm bleeder	Necessary	Not necessary



9 Pcs 22uF for 1.0MHz + 5 Pcs 22uF DY

Cymtec 6.8mm x7.6mmx3.0mm
OCR: 0.9m Ohm +/- 7%
Idc : 35A , Isat : 41A

Iccmax= 24A
TDC=4A

068.R1510.1171
2nd = 068.R1510.1141

79.3371V.2PL
2nd = 079.3371V.0031
PANASONIC
ESR: 9 mohm

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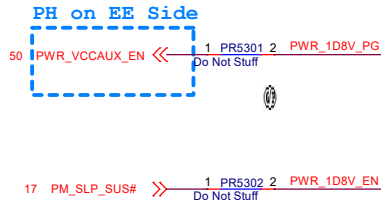
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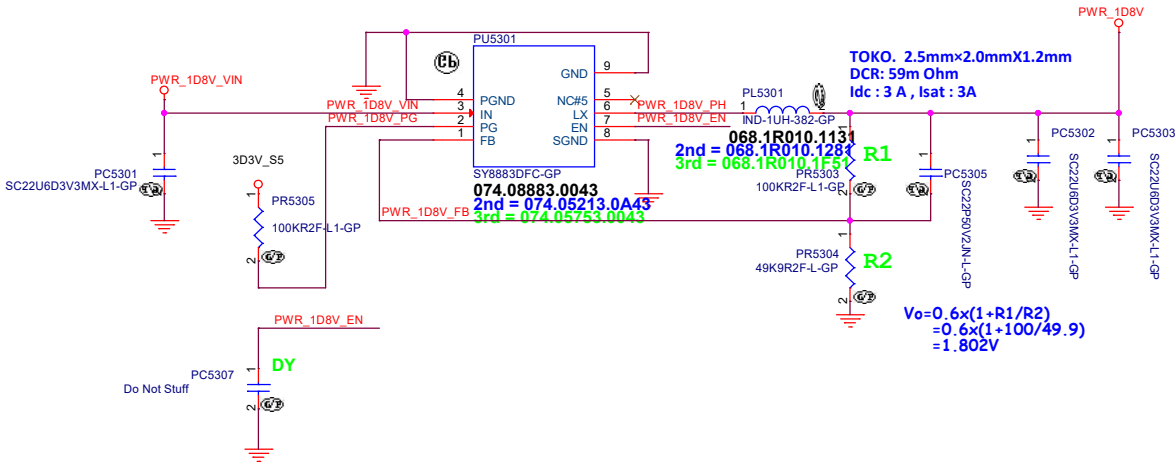
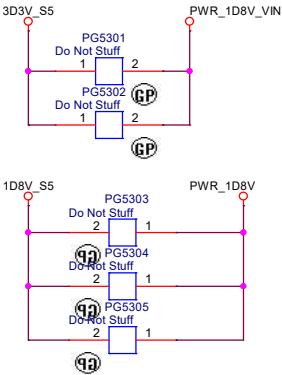
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Title <div>Power (RSVD)</div>		
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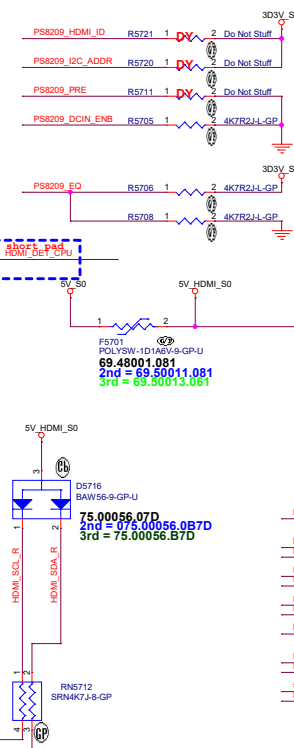
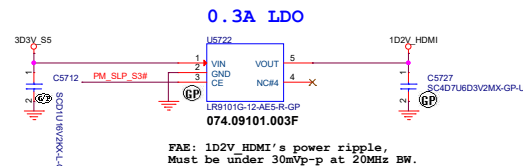
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Title <div>Display (RSVD)</div>		
Size <div>A4</div>	Document Number <div>Airking_JL</div>	Rev <div>-1</div>
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From GPU				To Repeater			
HDMI_DDI_TX_P0	C5701	1	2	SCD1U16/2X0X1-GP	HDMI_DDI_TX_C_P0		
HDMI_DDI_TX_N0	C5702	1	2	SCD1U16/2X0X1-GP	HDMI_DDI_TX_C_N0		
HDMI_DDI_TX_P1	C5703	1	2	SCD1U16/2X0X1-GP	HDMI_DDI_TX_C_P1		
HDMI_DDI_TX_N1	C5704	1	2	SCD1U16/2X0X1-GP	HDMI_DDI_TX_C_N1		
HDMI_DDI_TX_P2	C5705	1	2	SCD1U16/2X0X1-GP	HDMI_DDI_TX_C_P2		
HDMI_DDI_TX_N2	C5706	1	2	SCD1U16/2X0X1-GP	HDMI_DDI_TX_C_N2		
HDMI_DDI_TX_P3	C5707	1	2	SCD1U16/2X0X1-GP	HDMI_DDI_TX_C_P3		
HDMI_DDI_TX_N3	C5708	1	2	SCD1U16/2X0X1-GP	HDMI_DDI_TX_C_N3		

[illegible]

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Title <div>Display (RSVD)</div>		
Size <div>A4</div>	Document Number <div>Airking_JL</div>	Rev <div>-1</div>
Date: Tuesday, February 23, 2021		Sheet 58 of 106

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Title <div>Display (RSVD)</div>		
Size <div>A4</div>	Document Number <div>Airking_JL</div>	Rev <div>-1</div>
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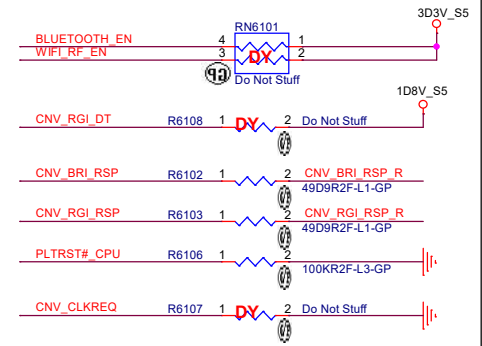
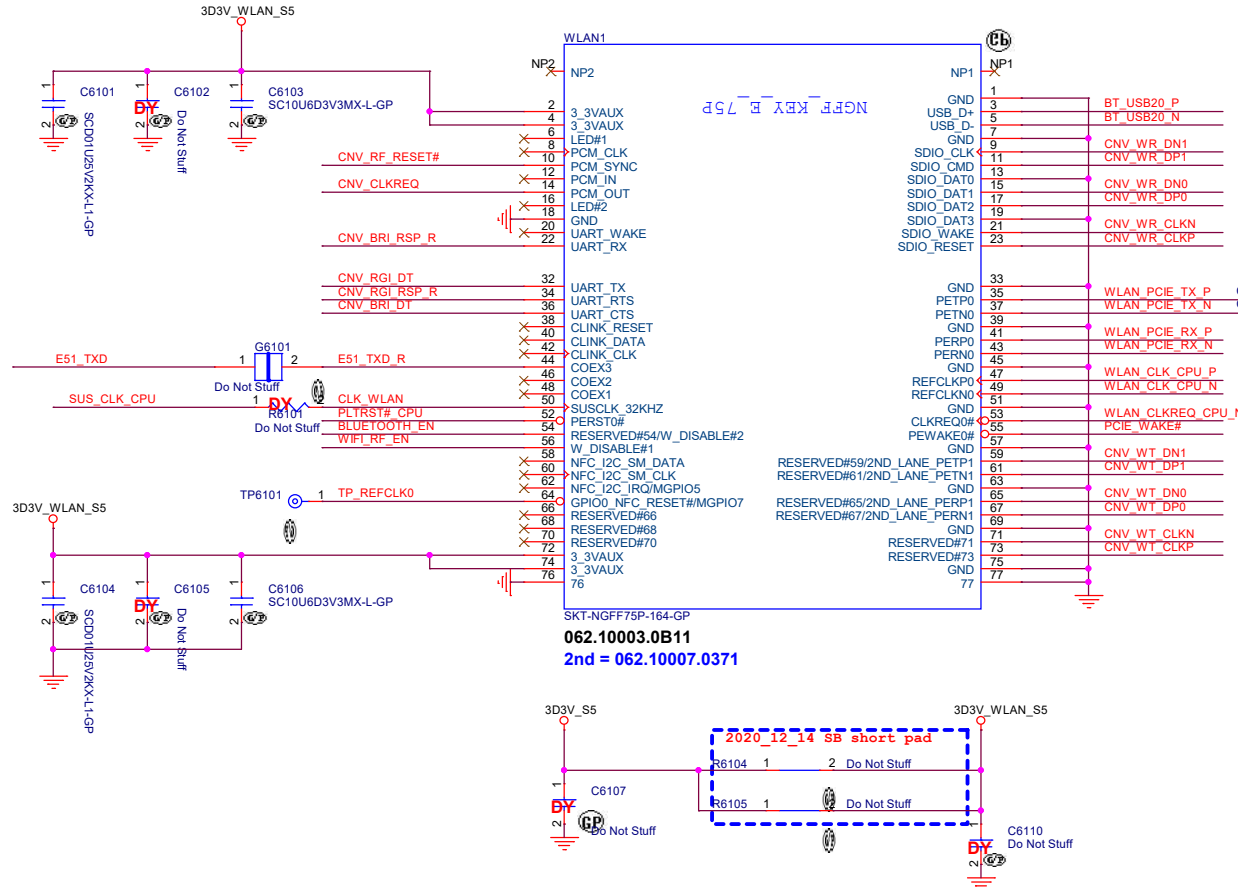
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Title			INT IO (RSVD)		
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SSID = Wireless

Mini Card Connector (802.11a/b/g/n)

- 19 CNV_RF_RESET#
- 19 CNV_CLKREQ
- 21 CNV_BRI_RSP
- 21 CNV_RGI_DT
- 21 CNV_RGI_RSP
- 21 CNV_BRI_DT
- 24,68 E51_TXD
- 18 SUS_CLK_CPU
- 17,63,89,91 PLTRST#_CPU
- 18,89 BLUETOOTH_EN
- 18,89 WIFI_RF_EN
- 16,89 BT_USB20_P
- 16,89 BT_USB20_N
- 21 CNV_WR_DN1
- 21 CNV_WR_DP1
- 21 CNV_WR_DN0
- 21 CNV_WR_DP0
- 21 CNV_WT_DN1
- 21 CNV_WT_DP1
- 21 CNV_WT_DN0
- 21 CNV_WT_DP0
- 21 CNV_WT_CLKN
- 21 CNV_WT_CLKP
- 16,89 WLAN_PCIE_TX_C_P
- 16,89 WLAN_PCIE_TX_C_N
- 16,89 WLAN_PCIE_RX_P
- 16,89 WLAN_PCIE_RX_N
- 18,89 WLAN_CLK_CPU_P
- 18,89 WLAN_CLK_CPU_N
- 18,89 WLAN_CLKREQ_CPU_N
- 17,63,89 PCIE_WAKE#
- 21 CNV_WT_DN1
- 21 CNV_WT_DP1
- 21 CNV_WT_DN0
- 21 CNV_WT_DP0
- 21 CNV_WT_CLKN
- 21 CNV_WT_CLKP



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Title			INT IO (WLAN M.2)	
Size	Document Number	A3 Airing_JL		Rev
Date:	Tuesday, February 23, 2021	Sheet	61	of 106
			-1	

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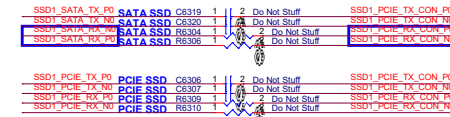
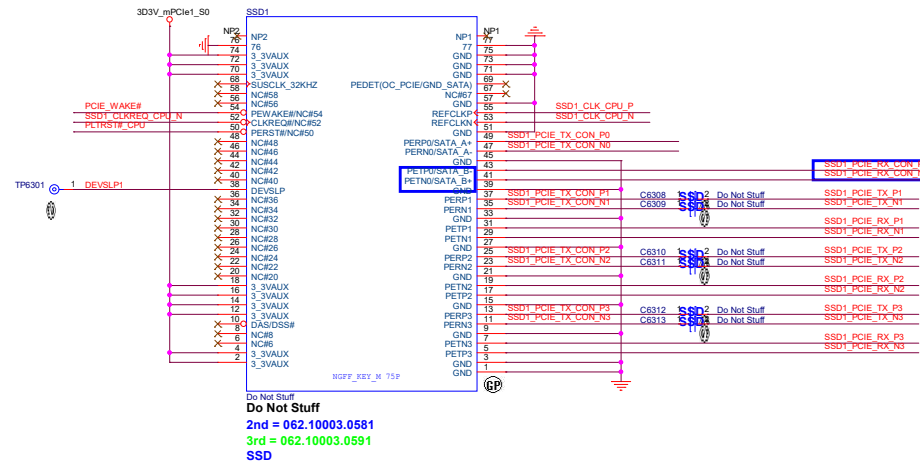
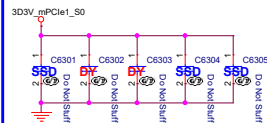
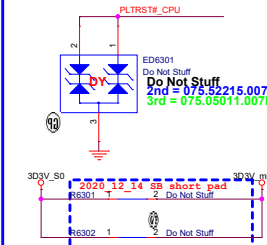
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Title (Reserved)			
Size A3	Document Number Airking_JL		Rev -1
Date: Tuesday, February 23, 2021	Sheet 62	of 106	1

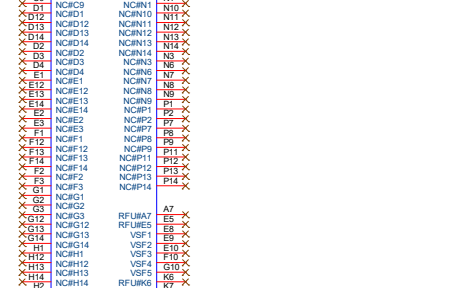
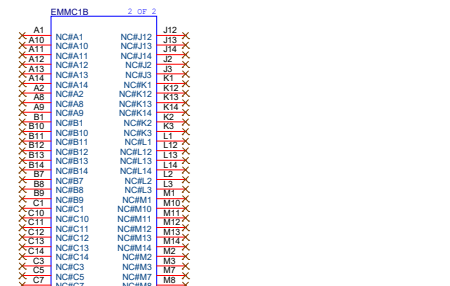
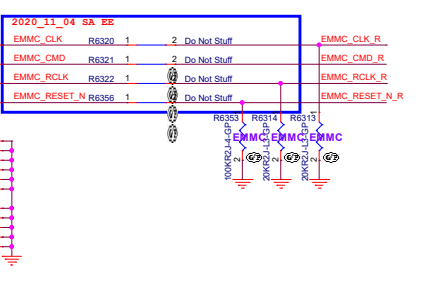
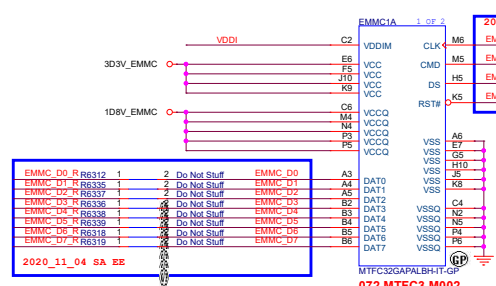
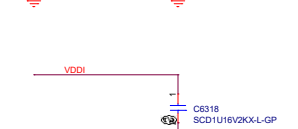
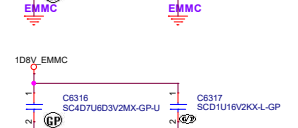
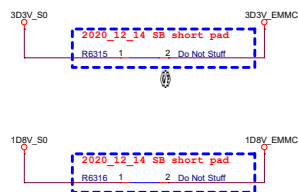
SSID = mPCIe Mini Card Connector

17.61.89 PCIE_WAKE# <<>
18 SSD1_CLKREQ_CPU_N <<>
17.61.89.91 PLTRST#_CPU <<>
16 DEVSUP1 <<>



SSID = eMMC

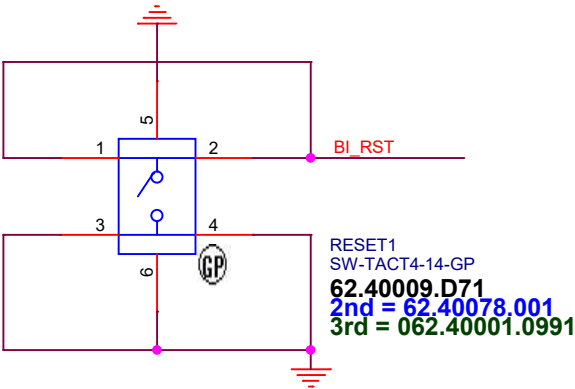
96 EMMC_CLK
96 EMMC_CMD
21.96 EMMC_CLK_R
21.96 EMMC_CMD_R
21 EMMC_RCLK_R
21 EMMC_D0_R
21 EMMC_D1_R
21 EMMC_D2_R
21 EMMC_D3_R
21 EMMC_D4_R
21 EMMC_D5_R
21.96 EMMC_D0_R
21.96 EMMC_D1_R
21.96 EMMC_D2_R
21.96 EMMC_D3_R
21.96 EMMC_D4_R
21.96 EMMC_D5_R
96 EMMC_D0
96 EMMC_D1
96 EMMC_D2
96 EMMC_D3
96 EMMC_D4
96 EMMC_D5



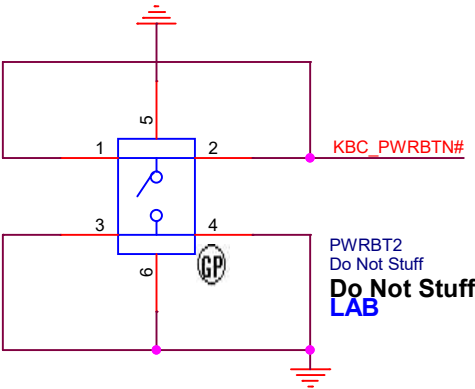
43,89 BI_RST
24,66,89 KBC_PWRBTN#



Battery Reset

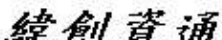


Power Button



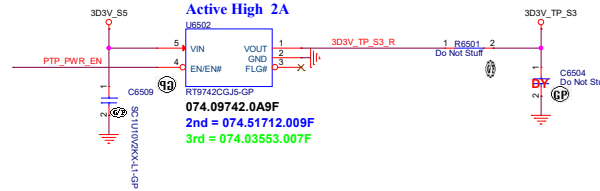
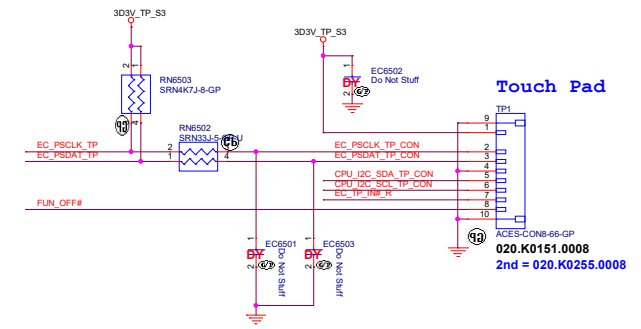
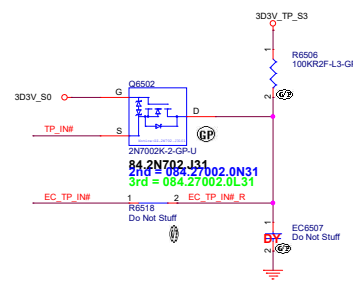
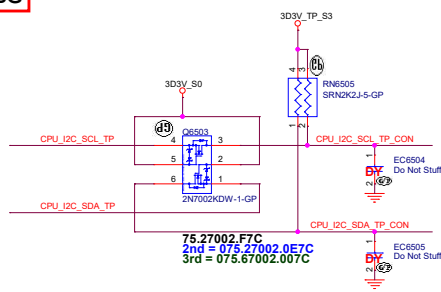
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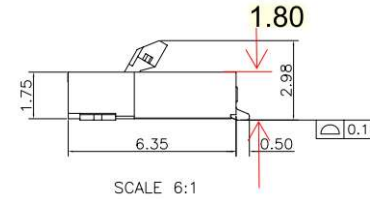
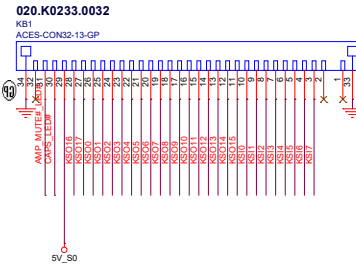
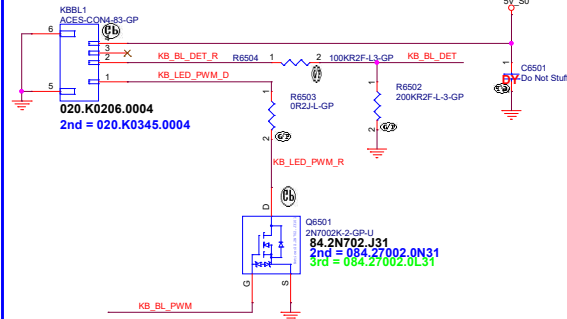
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
LED / Button / Power Button			
Size A4	Document Number Airking_JL		Rev -1
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SSID = KBC

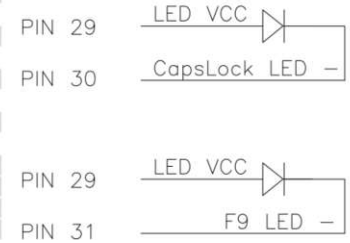
20.96 CPU_I2C_SCL_TP
20.96 CPU_I2C_SDA_TP
21 TP_IN#
24 EC_TP_IN#
24 PTP_PWR_EN
24 EC_PCLK_TP
24 EC_PSDAT_TP
24.89 FUN_OFF#
89 EC_PCLK_TP_CON
89 EC_PSDAT_TP_CON
89.96 CPU_I2C_SDA_TP_CON
89.96 CPU_I2C_SCL_TP_CON
89 EC_TP_IN#_R



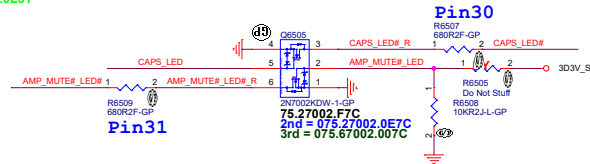
Internal KeyBoard Connector



1	NC
2	NC
3	C08
4	C07
5	C06
6	C05
7	C04
8	C03
9	C02
10	C01
11	R16
12	R15
13	R14
14	R13
15	R12
16	R11
17	R10
18	R09
19	R08
20	R07
21	R06
22	R05
23	R04
24	R03
25	R02
26	R01
27	R18
28	R17
29	LED VCC
30	CapsLock LED -
31	F9 LED -
32	NC



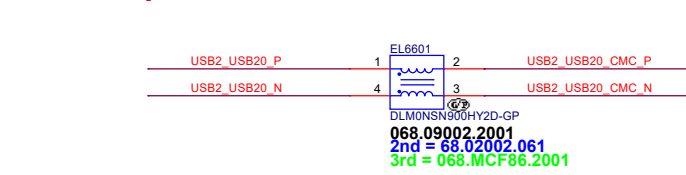
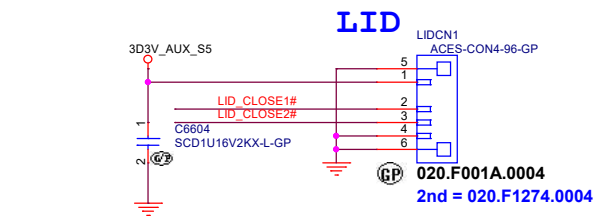
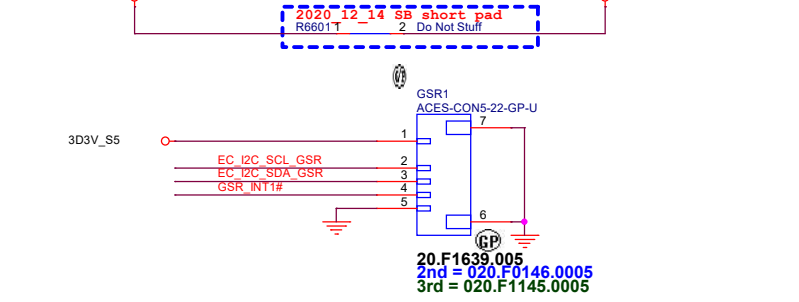
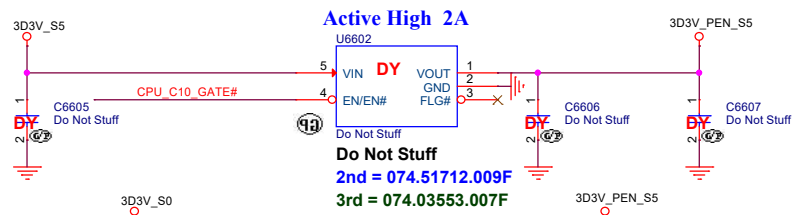
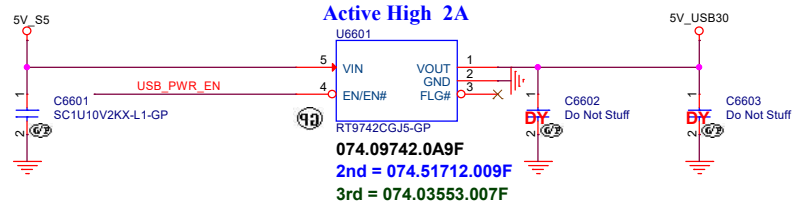
24.89 KSO0
24.89 KSO1
24.89 KSO2
24.89 KSO3
24.89 KSO4
24.89 KSO5
24.89 KSO6
24.89 KSO7
24.89 KSO8
24.89 KSO9
24.89 KSO10
24.89 KSO11
24.89 KSO12
24.89 KSO13
24.89 KSO14
24.89 KSO15
24.89 KSO16
24.89 KSO17
24.89 KSI0
24.89 KSI1
24.89 KSI2
24.89 KSI3
24.89 KSI4
24.89 KSI5
24.89 KSI6
24.89 KSI7
24 KB_BL_DET
24 KB_BL_PWM
89 KB_BL_DET_R
89 KB_LED_PWM_D
24 CAPS_LED
27 AMP_MUTE#_LED



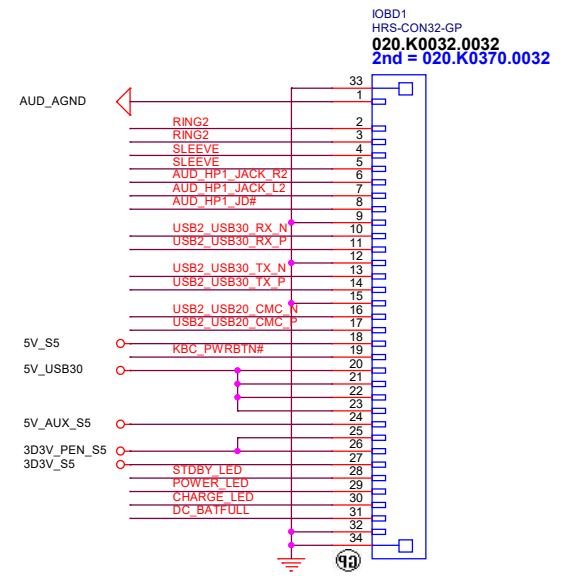
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SSID = User.Interface

- 27.89 RING2
- 27 SLEEVE
- 27.89 AUD_HP1_JACK_R2
- 27.89 AUD_HP1_JACK_L2
- 27 AUD_HP1_JD#
- 24 USB_PWR_EN
- 16 USB2_USB30_RX_N
- 16 USB2_USB30_RX_P
- 16 USB2_USB30_TX_N
- 16 USB2_USB30_TX_P
- 16.89 USB2_USB20_N
- 16.89 USB2_USB20_P
- 17.40 CPU_C10_GATE#
- 24.64.89 KBC_PWRBTN#
- 24.89 STDBY_LED
- 24.89 POWER_LED
- 24.89 CHARGE_LED
- 24.89 DC_BATFULL
- 24.89 LID_CLOSE1#
- 24.89 LID_CLOSE2#
- 24.70 GSR_INT1#
- 24.70.96 EC_I2C_SDA_GSR
- 24.70.96 EC_I2C_SCL_GSR



IOBD1:
5V_USB30 for USB 3.0
5V_AUX_S5 & 5V_S5 for LED
3D3V_PEN_S5 for PEN
3D3V_S5 for USB3.0 ReDriver



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Title <div>Sensor (RSVD)</div>		
Size <div>A4</div>	Document Number <div>Airking_JL</div>	Rev <div>-1</div>
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Title <div>Sensor (RSVD)</div>		
Size <div>A4</div>	Document Number <div>Airking_JL</div>	Rev <div>-1</div>
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SSID = G Sensor

The default I²C address of the device is 0011000b (0x18). It is used if the SDO pin is pulled to 'GND'. The alternative address 0011001b (0x19) is selected by pulling the SDO pin to 'V_{DDIO}'.

Note

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

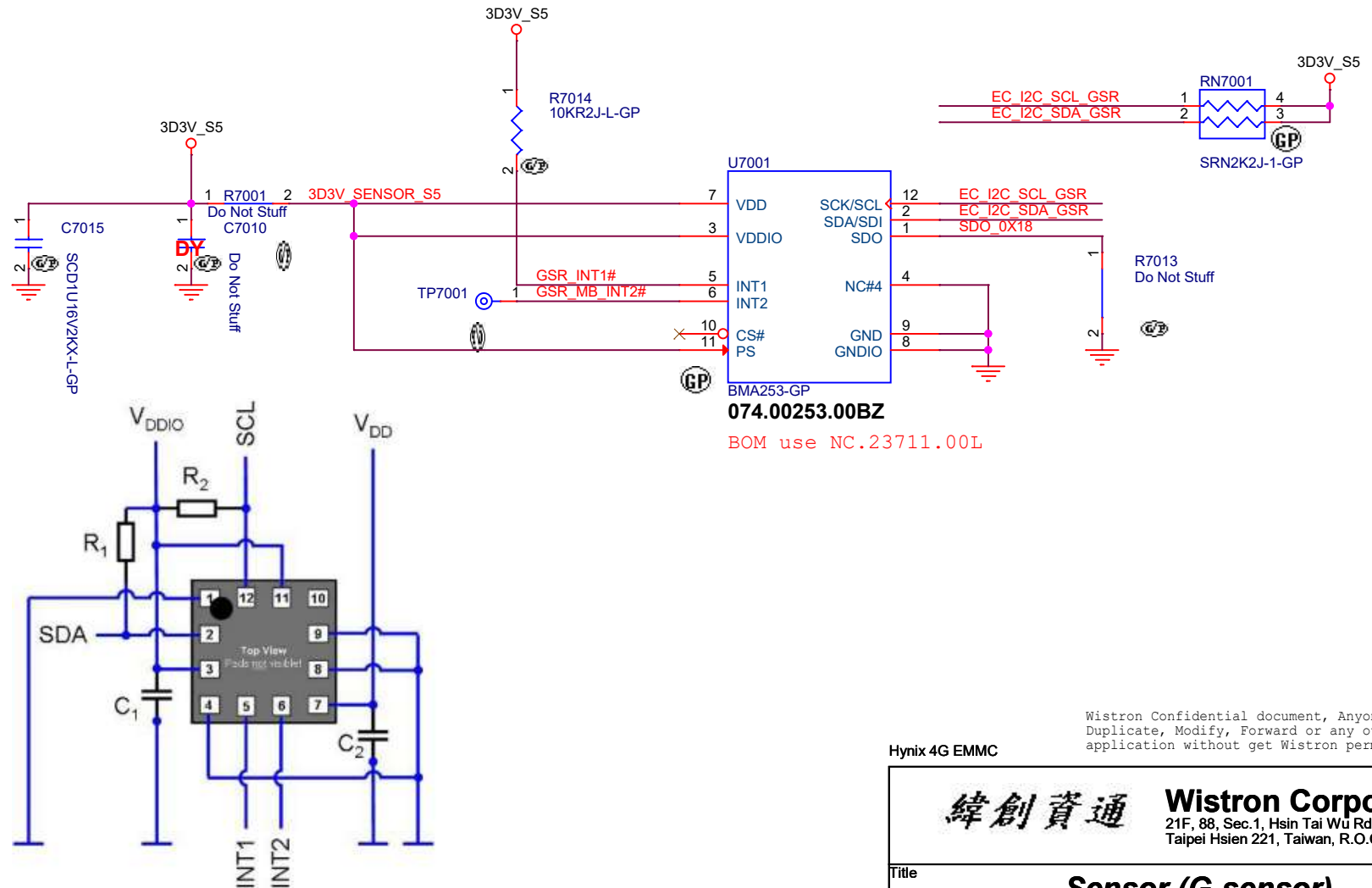


Figure 26: I²C connection

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Title

Sensor (G-sensor)

Size

Document Number

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Title

EXT IO (RSVD)

Size

Document Number

Rev

A3

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Date

Tuesday, February 23, 2021

Sheet

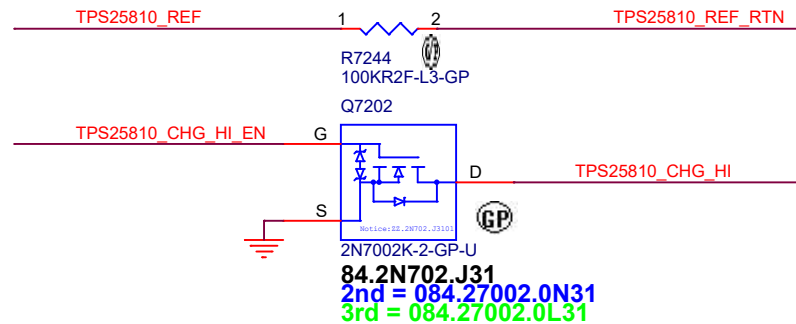
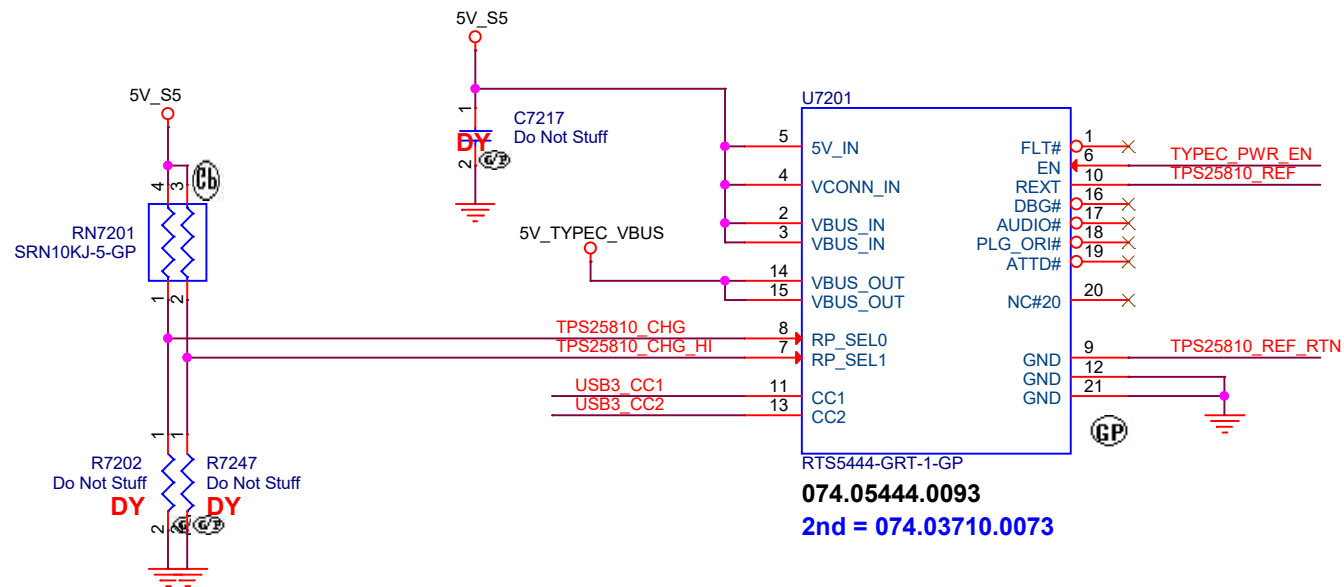
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of

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24 TPS25810_CHG_HI_EN >>—
 24 TYPEC_PWR_EN >>—
 73 USB3_CC1 <<<—
 73 USB3_CC2 <<<—



CHG	CHG_HI	CC Capability Broadcast	Current Limit	Load Detect Threshold
0	0	STD	1.67 A	NA
0	1	STD	1.67 A	NA
1	0	1.5 A	1.67 A	NA
1	1	3.0 A	3.34 A	1.77 A

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Title	
EXT IO (Type C CC Logic)	
Size A4	Document Number Airking_JL
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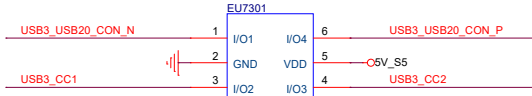
USB HOST

16 USB3_USB20_N
16 USB3_USB20_P
16 USB3_USB30_TX_P0
16 USB3_USB30_TX_N0
16 USB3_USB30_RX_P0
16 USB3_USB30_RX_N0
16 USB3_USB30_TX_P1
16 USB3_USB30_TX_N1
16 USB3_USB30_RX_P1
16 USB3_USB30_RX_N1

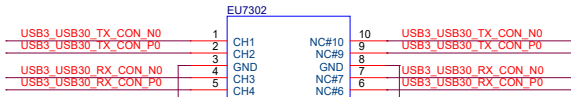
72 USB3_CC1
72 USB3_CC2



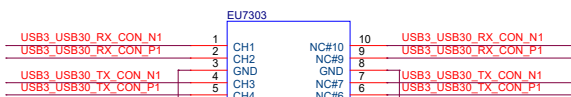
DLM0NSN900HY2D-GP
068.09002.2001
2nd = 68.02002.061
3rd = 068.MCF86.2001



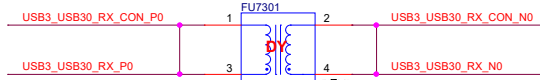
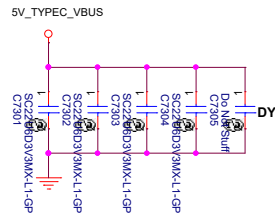
AZC099-04S-2-GP
075.09904.0A7C
2nd = 075.53456.000C
3rd = 075.54236.007C



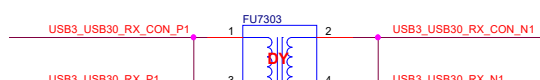
PUSB3FR4Z-GP
075.PUSB3.0A73
2nd = 075.73034.0073
3rd = 075.00176.0073



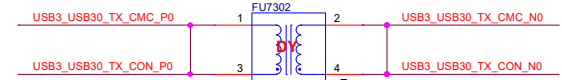
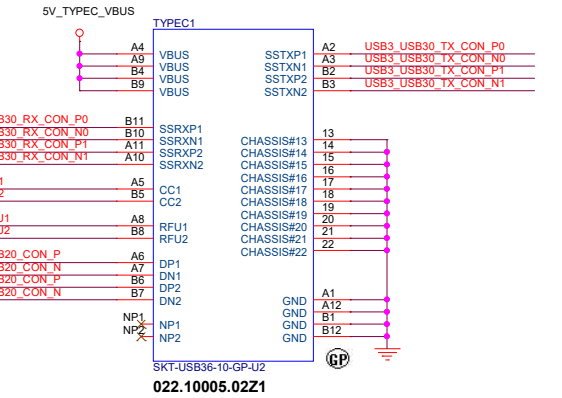
PUSB3FR4Z-GP
075.PUSB3.0A73
2nd = 075.73034.0073
3rd = 075.00176.0073



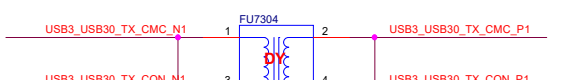
Do Not Stuff
2nd = 068.10129.2021
3rd = 068.01210.2031



Do Not Stuff
2nd = 068.10129.2021
3rd = 068.01210.2031



Do Not Stuff
2nd = 068.10129.2021
3rd = 068.01210.2031



Do Not Stuff
2nd = 068.10129.2021
3rd = 068.01210.2031

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Title EXT IO (USB_Type_C)
Size Custom Document Number Airking_JL Rev -1
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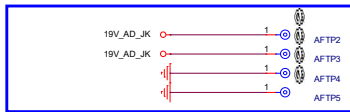
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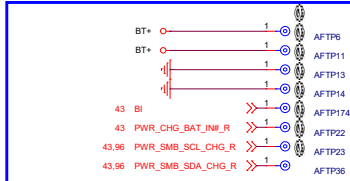
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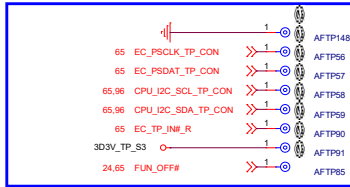
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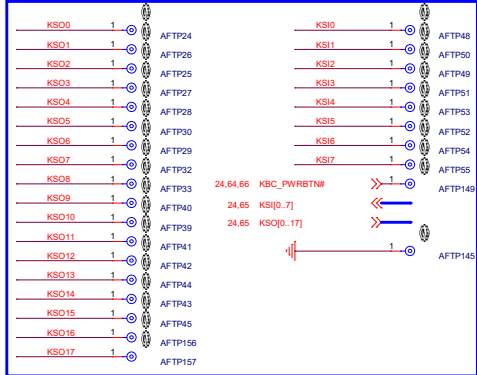
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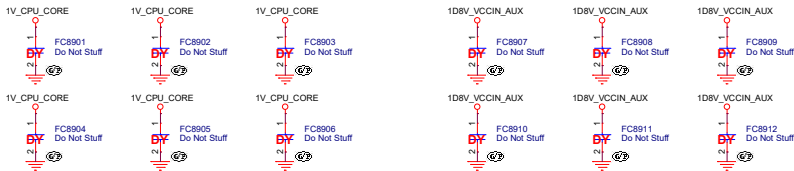
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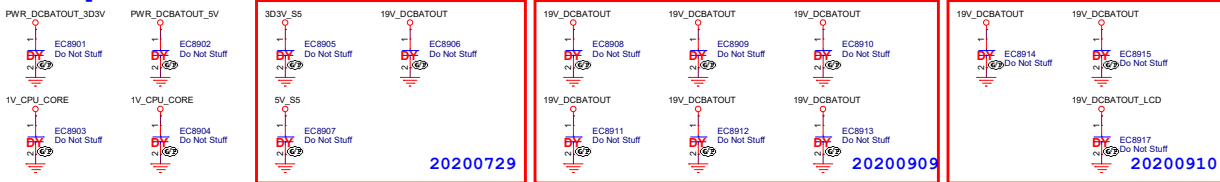
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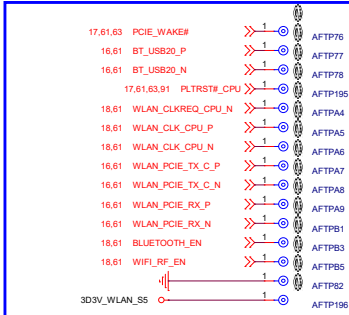
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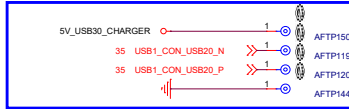
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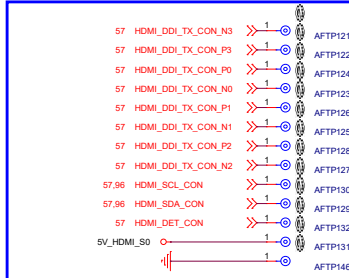
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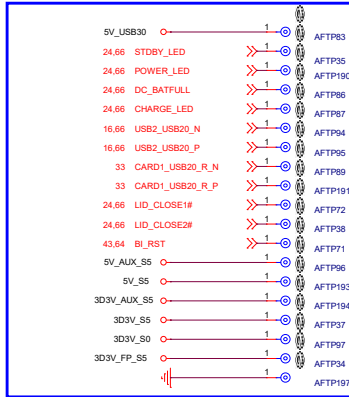
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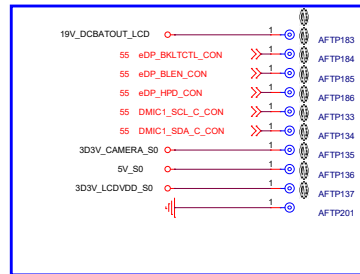
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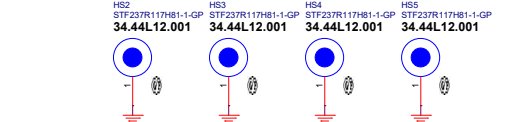
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LCD1



Stand off 1



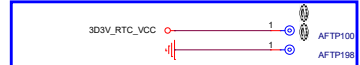
Screw pad



KBBL1



RTC1



AUDIO1



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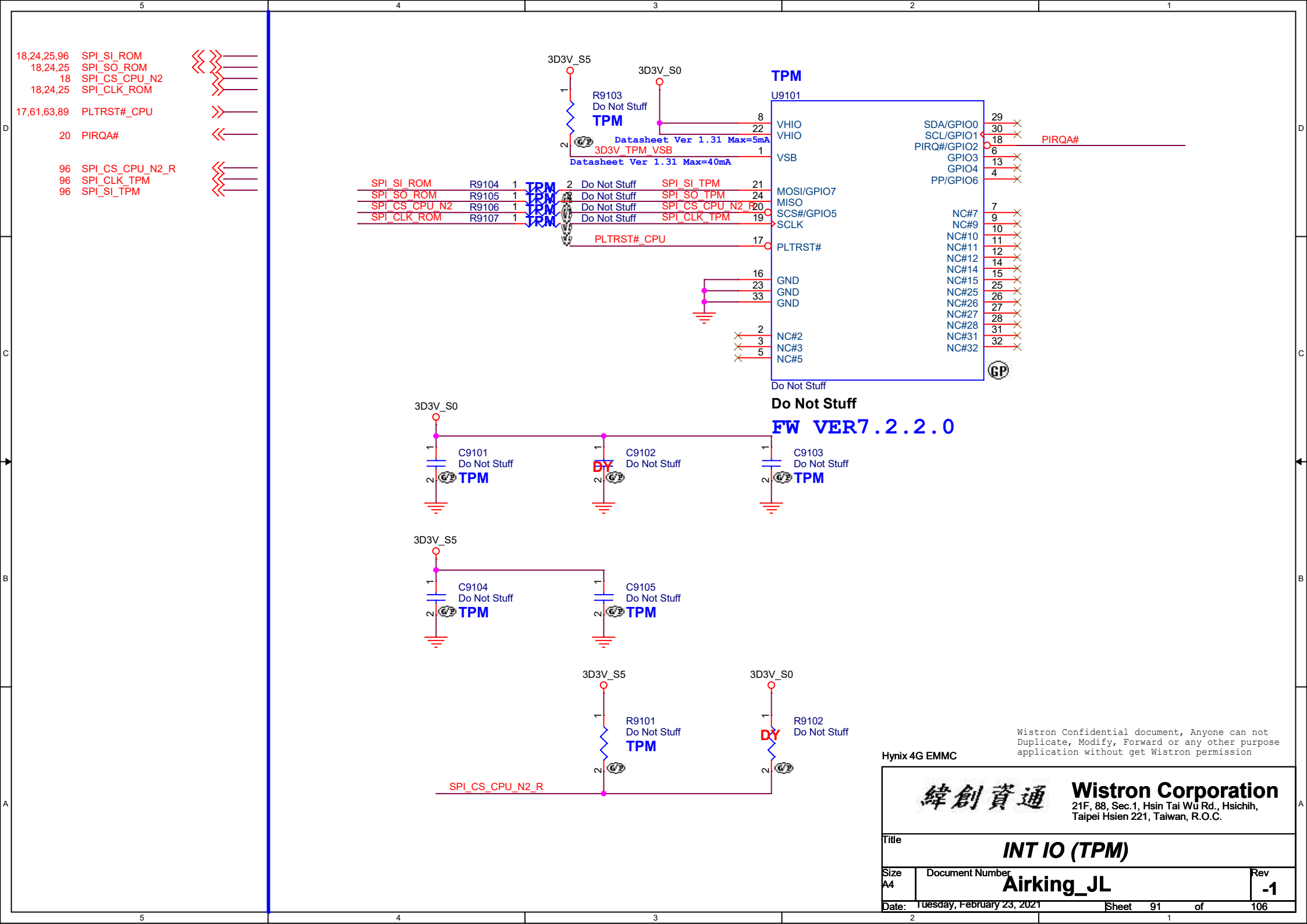
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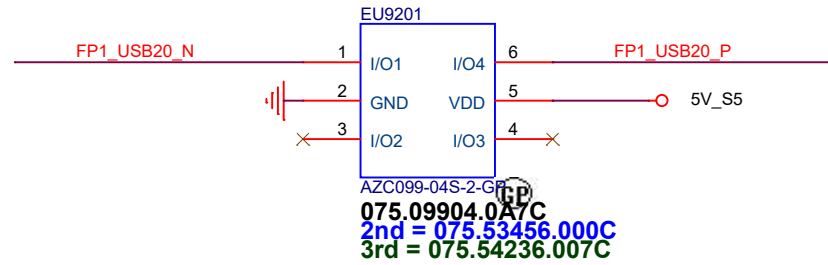
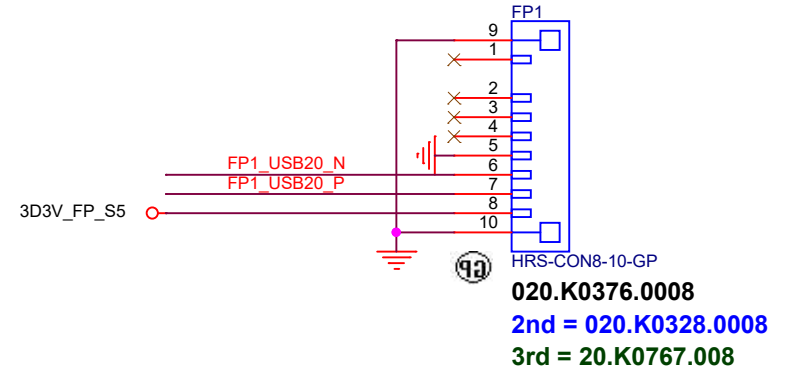
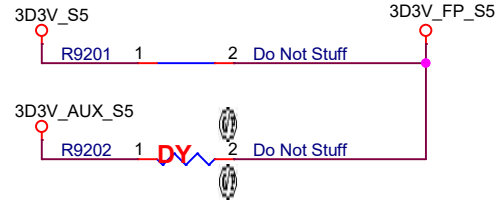
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16 FP1_USB20_N
16 FP1_USB20_P



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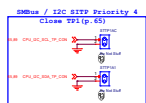
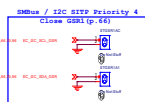
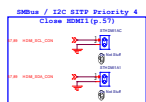
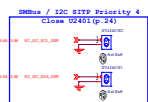
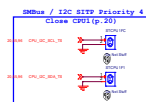
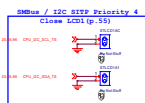
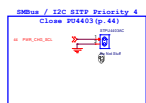
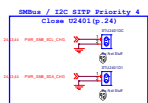
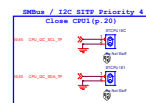
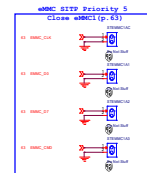
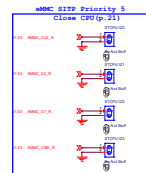
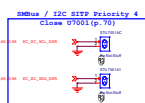
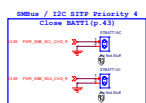
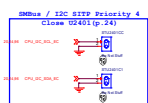
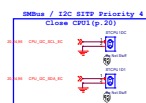
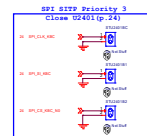
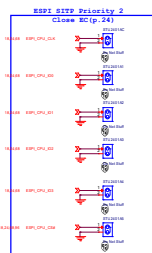
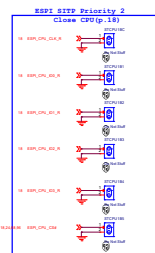
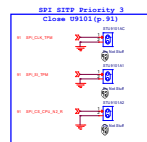
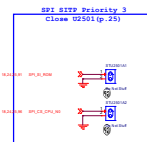
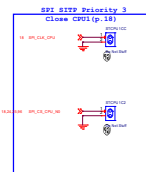
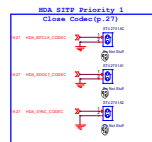
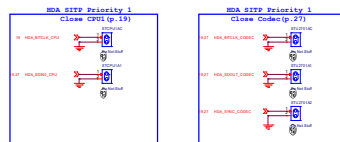
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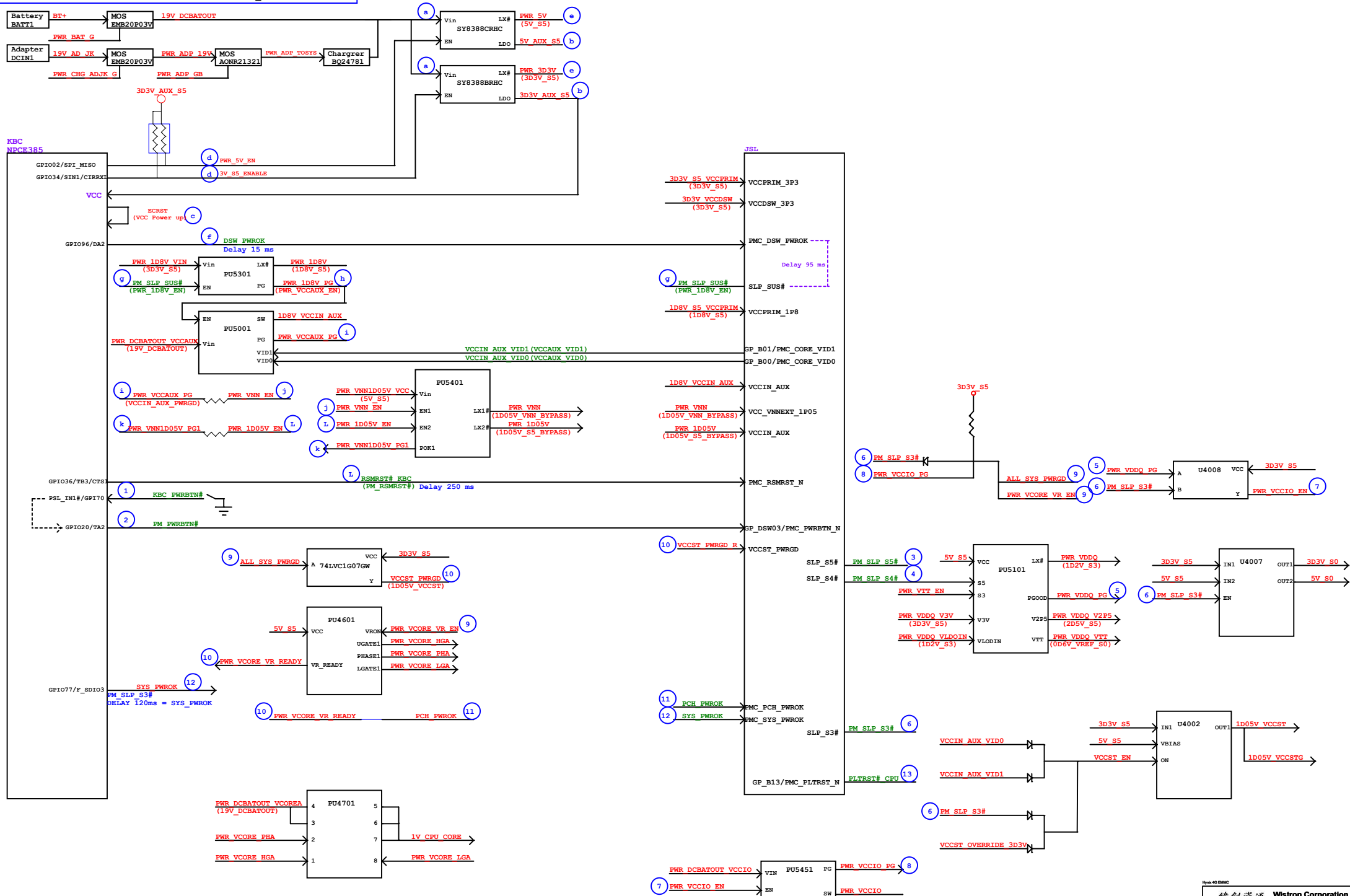
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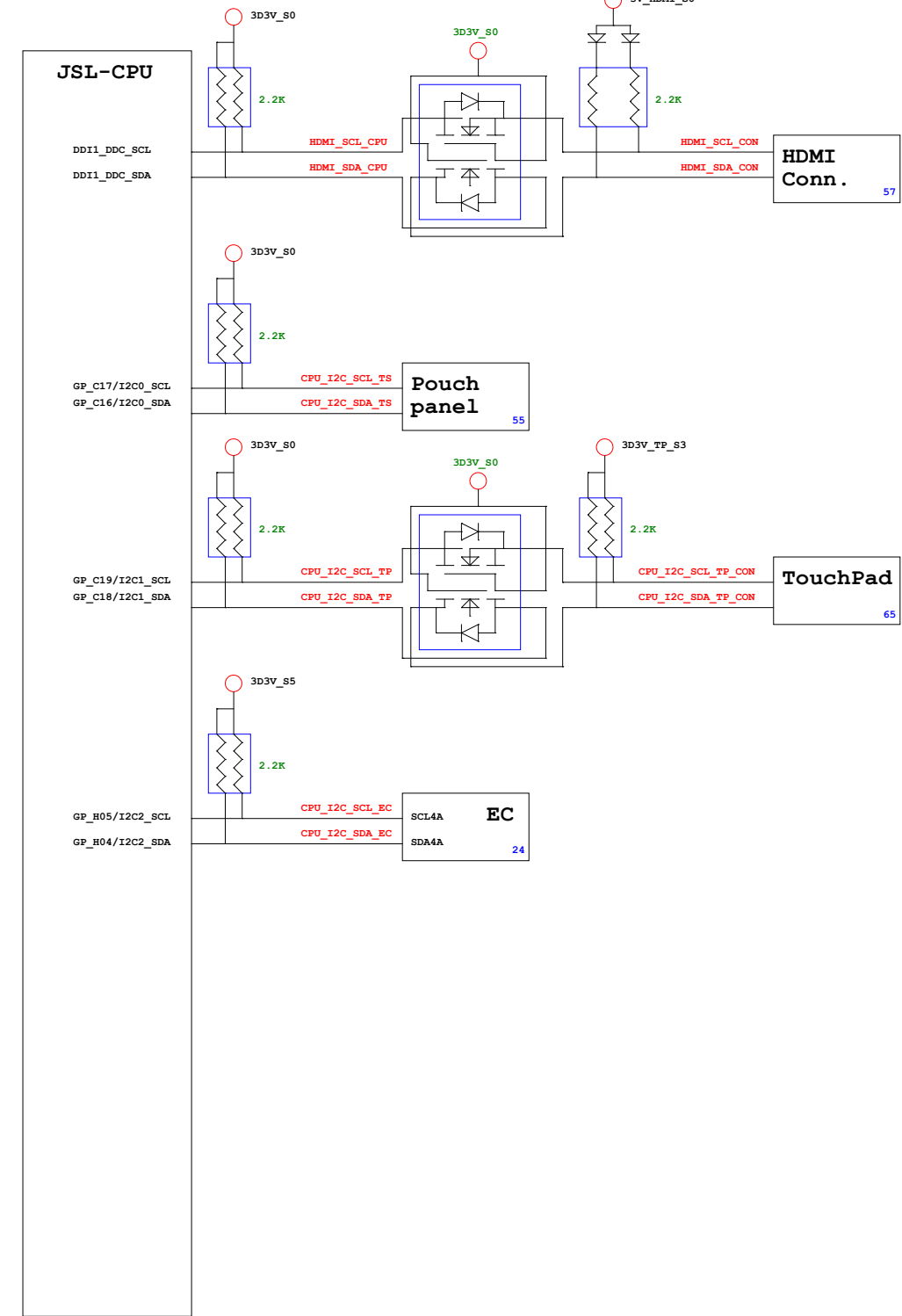
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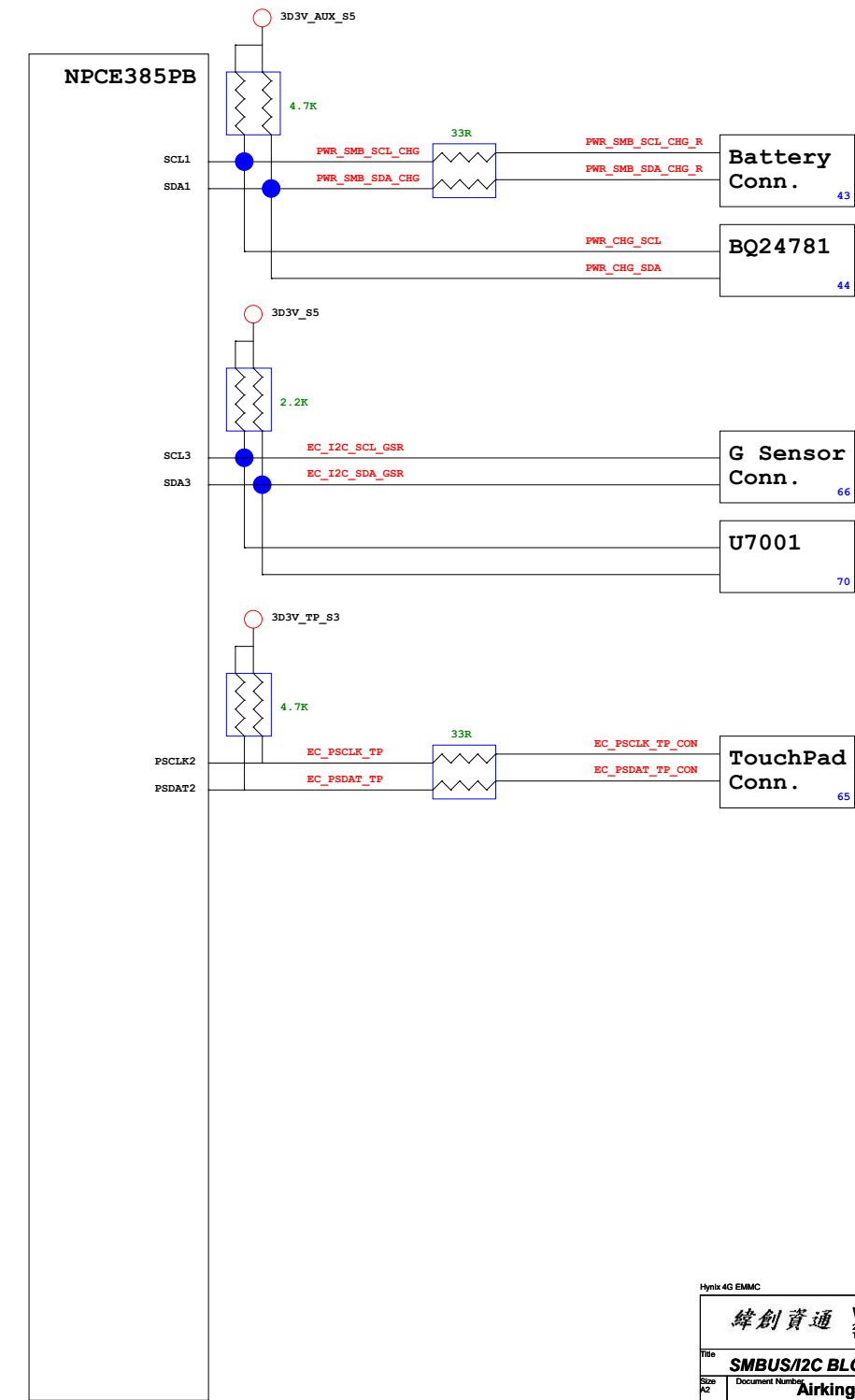
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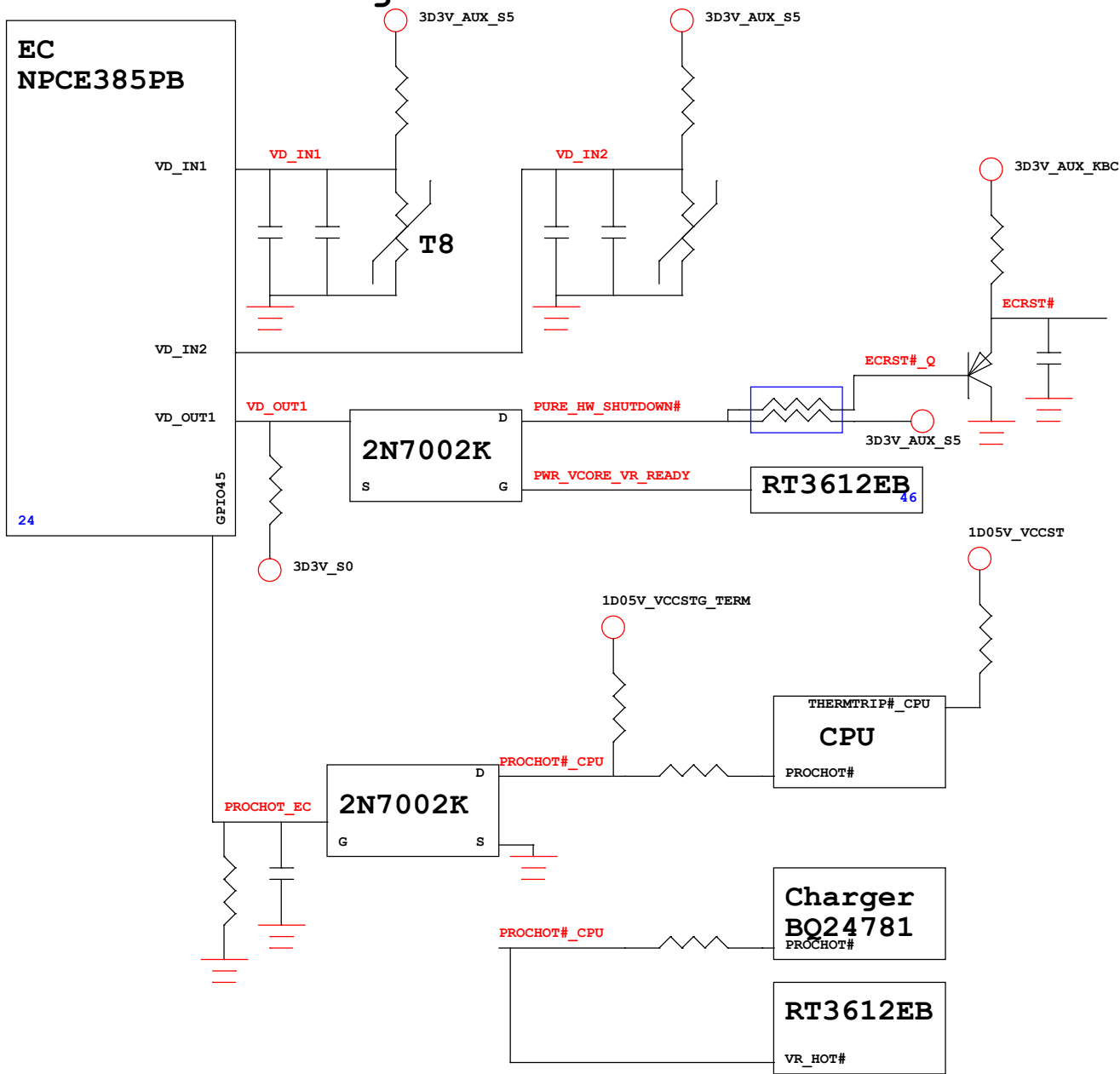
SOC SMBus/I2C Block Diagram



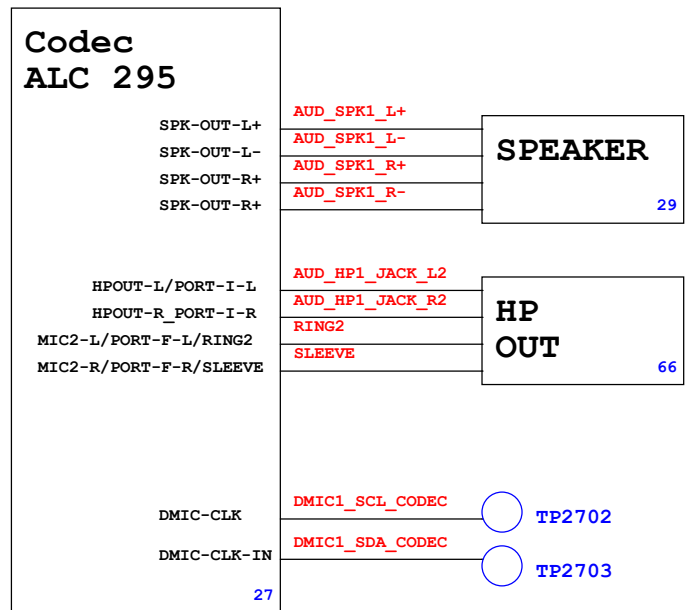
EC SMBus/I2C Block Diagram



Thermal Block Diagram



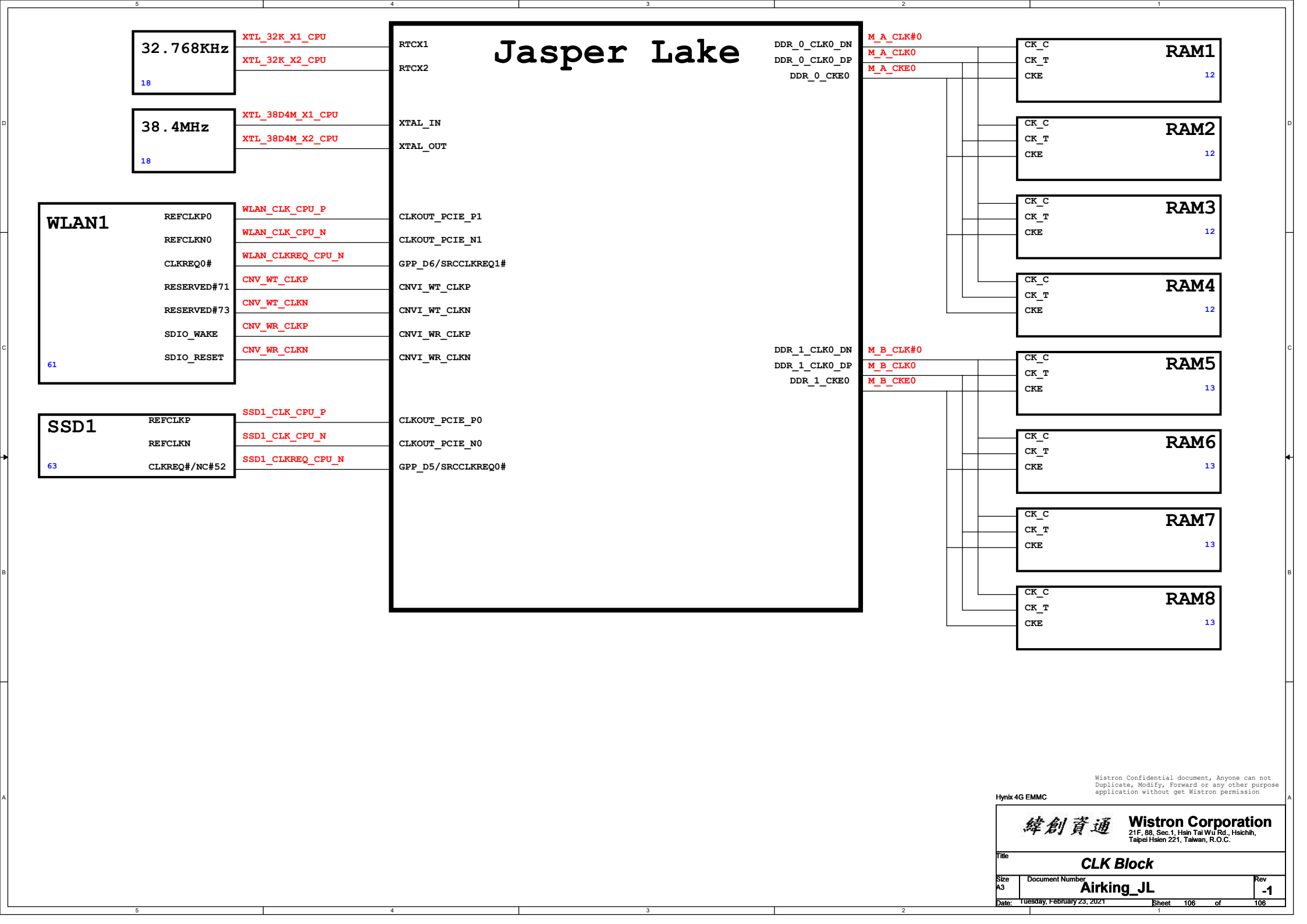
Audio Block Diagram



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Hynix 4G EMMC

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